IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2014 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 9, 10, 11, 12, 13

CONFERENCE THEME:

SILICON SYSTEMS BRIDGING THE CLOUD

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
PLENARY ROUNDTABLE ON THE FUTURE
CEO/VC PANEL ON THE FUTURE

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: Digital Assisted Analog & Analog Assisted Digital Techniques; 3D for Imagers & Memory

10 TUTORIALS: Transceiver Filtering; V_{min} Contstraints & Optimzation; 3D Power & Contactless Coupling; Power Optimized Processors; ADC Peripheral Circuits; Gb/s Receiver Front-Ends; Adaptive Processor Powering; Interference-Robust Receivers; Charge-Pump Converters; Physical-to-Digital Converters

2 EVENING EVENTS: Graduate-Student Research in Progress; Data Centers for the Cloud

THURSDAY ALL-DAY

4 FORUMS: Adpative Design for Energy Efficiency; mm-Waves in Safety & Communication; Low Power Sensor Radio; Future Energy Efficient I/O

SHORT-COURSE:
Biomedical and Sensor Interface Circuits

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at thecutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 9th**, the day before the official opening of the Conference, ISSCC 2014 offers:

- A choice of up to 4 of a total of 10 Tutorials
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, "**Data Centers to Support Tomorrow's Cloud**" will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a Distinguished member of the solid-state circuit community.

On **Monday, February 10th**, ISSCC 2014 offers four plenary papers on the theme: "**Silicon Systems Bridging the Cloud**". On Monday at 12:15 pm, there will be a Women's Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with the Book Display and Author Interviews, will also include a **Demonstration Session**, featuring posters and live demonstrations for selected papers from industry and academia. Monday evening will feature 6 distinguished researchers in a Plenary Roundtable discussion on "**Next-Generation Networked Systems "Challenges for Silicon"**.

On **Tuesday, February 11th**, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with the Book Display and Author Interviews. Tuesday evening sessions include two evening panels on "**Anatomy of Innovation: Bug or Feature**?", and "**Perspectives on the Future of Semiconductor Innovation**", as well as one Special-Topic Session on "**Wearable Wellness Devices: Fashion, Health, and Informatics**".

On **Wednesday, February 12th**, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On **Thursday, February 13th**, ISSCC offers a choice of five all-day events:

- A Short Course on "**Biomedical and Sensor Interface Circuits**"
- Four Advanced-Circuit-Design Forums on
  "**Adaptive Design Techniques for Energy Efficiency**";
  "**mm-Wave Advances for Active Safety & Communication Systems**";
  "**Low Power Radios for Sensor Networks**";
  "**Energy Efficient I/O Design for Next-Generation Systems**"

Registration for educational events on Sunday and Thursday will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

TABLE OF CONTENTS

T1: Filtering in RF Transceivers

Filtering is a fundamental function performed by RF transceivers. This tutorial starts with a review of filtering requirements for modern RF receivers and presents a review of traditional and recently rediscovered filtering techniques. Design of passive switched-capacitor filters is covered in detail along with recently rediscovered N-path filters. Examples of filter designs are provided.

Instructor: Borivoje Nikolic

Borivoje Nikolic is a Professor of Electrical Engineering and Computer Science at the University of California, Berkeley and a Scientific Co-Director of the Berkeley Wireless Research Center. He received the Ph.D. degree from the University of California at Davis in 1999. Dr. Nikolic has received best paper awards at ISSCC, the Symposium on VLSI Circuits, the IEEE International SOI Conference, the European Solid-State Device Research Conference, and ACM/IEEE ISLPE.

T2: V_{min} Constraints and Optimization in VLSI Circuit Design

With growing demand for energy efficiency, the ability to achieve lower minimum operating voltages (V_{min}) will be a key enabler in future VLSI systems. V_{min} for a given design depends on factors such as performance and energy targets, variability margins, and package limitations, the relative importance of which can vary widely between applications. This tutorial reviews V_{min} constraints that are relevant to VLSI circuit designers and summarizes methods to overcome these issues to improve V_{min}. Topics to be covered include V_{min} constraints and optimization techniques spanning frequency, functionality, package, energy/op, and reliability considerations.

Instructor: Leland Chang

Leland Chang received the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley and joined the IBM T. J. Watson Research Center in 2003, where he is now Manager of Design and Technology Solutions. His work focuses on power efficiency in high-performance systems, spanning the development of new technology elements, the design of high-performance memory and power management circuits, and the exploration of novel accelerator and memory system architectures. Key contributions include early demonstration of the FinFET structure for CMOS scaling, 8T-SRAM for voltage scaling in high-performance caches, high-speed register files with double-pumped access ports, and high-efficiency voltage conversion circuits using new passive device technologies. He is the author of 69 technical articles and 56 patents and is currently a member of the ISSCC technical program committee.

T3: 3D Integration, Power Delivery, and Contactless Interconnect by Near-Field Coupling

Data communication and power transfer by using near-field coupling have gained increasing attention as an attractive technology direction. With the recent introduction of standards for next-generation memory interfaces (Wide IO) and wireless power transfer (Qi), the commercial adoption of these technologies is progressing. Research on non-contact connecters using electromagnetic coupling has also started. In this tutorial, we introduce the basics of near-field coupling, together with circuit implementations, and applications to the following areas: (1) Wide IO for die stacking by inductive coupling (compared with TSV), (2) Power transfer by inductive coupling and magnetic resonant coupling, and (3) Connectors for reliable and compact assembly by electromagnetic coupling.

Instructor: Tadahiro Kuroda

Tadahiro Kuroda received the Ph.D. degree in Electrical Engineering from the University of Tokyo. In 1982, he joined Toshiba Corporation. In 2000, he moved to Keio University, where he has been a Professor since 2002. He was a Visiting MacKay Professor at the University of California, Berkeley in 2007. His research interests include low-power CMOS design, proximity communications and image recognition. He has published more than 200 papers, including 34 ISSCC papers, 21 VLSI Symposia papers, 19 CICC papers, and 16 A-SSCC papers. He wrote 22 books/chapters and filed >100 patents. He is an IEEE Fellow and an IEICE Fellow.

T4: Power-Optimized Processor Design

An increasing focus on design productivity is causing a gradual shift in the microprocessor design flow from custom design to synthesis-based methodologies. This reduces the power-optimization opportunities offered by previously developed custom-circuit-tuning techniques. This tutorial gives an overview of power-reduction techniques used in microprocessors, with a particular focus on digital design. It covers newly developed methodologies that emphasize broad design-space exploration to optimize designs for power at the structural level allowed by recent advances in the synthesis tools, and discusses the shift in the role and responsibilities of logic and circuit designers in the power-optimization efforts. In the summary, the tutorial shows how the power-optimization efforts across design disciplines come together in delivering a competitive product meeting power, performance and power-frequency limited yield goals.

Instructor: Victor Zyuban

Dr. Zyuban received a Ph.D. degree in Computer Science and Engineering from the University of Notre Dame. He joined the IBM T.J. Watson Research Center in 2000, where is he a Research Staff Member and manager. Within IBM, he is currently the pSeries server processor power lead. In this role, which he has held over the past 7 years, his responsibilities include leading the processor power-optimization and power-modeling flow, modeling the chip frequency and the Power-Frequency-Limited Yield (PFLY), as well as the chip power/frequency hardware-to-model correlation. Victor also leads several research projects in the area of low-power design at the IBM T.J. Watson Research Center. He has over 30 publications and more than 30 patents issued or filed.

T5: Peripheral Circuits for Analog-to-Digital Converters

The performance of modern analog-to-digital converters is often limited by the circuitry surrounding them. This tutorial explains how we measure analog-to-digital converters to ensure that we are not measuring the test equipment, and goes into detail on various circuit techniques often applied to ensure we get the best performance. I discuss topics ranging from DC precision to low-distortion RF. The digital side of an ADC often produces measurement artefacts and I describe common approaches to mitigate these issues. The firehose of data coming out of a GS/s ADC is a significant challenge when dealing with such devices. The tutorial helps both board-level engineers and chip designers to overcome issues that may limit circuit performance.

Instructor: Marco Corsi

Marco Corsi joined Texas Instruments in 1990. Shortly after, he designed breakthrough linear innovations including PCMCIA distribution switches, RS485 drivers, and custom PMICs for the then-new mobile phone industry. Marco led the high-speed ADC design group at Texas Instruments. He is responsible for many industry firsts including a 16b 200MS/s ADC as well as the first monolithic 12b 1GS/s ADC. He was elected TI Senior Fellow in 2013 and IEEE Fellow in 2012. Corsi earned a BA and MA from the University of Cambridge in England and holds 76 US patents.

T6: Analog Front-End Design for Gb/s Wireline Receivers

This tutorial introduces the design, analysis, and optimization of analog front-ends for state-of-the-art Gb/s wireline receivers. Specifically, the tutorial highlights key circuit/system requirements, tradeoffs, and gotchas inherent in the design of such receivers. In addition, the tutorial develops simple analytical formulas that accurately predict the power and performance characteristics of key circuit blocks such as continuous-time linear equalizers and decision-feedback equalizers.

Instructor: Elad Alon

Elad Alon received the Ph.D. degree in Electrical Engineering from Stanford University, Stanford, CA, in 2006. In 2007, he joined the University of California, Berkeley, where he is now an Associate Professor of Electrical Engineering and Computer Sciences, as well as a Co-Director of the Berkeley Wireless Research Center (BWRC). He has held consulting or visiting positions at Cadence, Xilinx, Wilocity, Oracle, Intel, AMD, Rambus, Hewlett Packard, and IBM

Research. His research focuses on energy-efficient integrated systems, including the circuit, device, communication, and optimization techniques used to design them. He received the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award, and the 2010 UC Berkeley Electrical Engineering Outstanding Teaching Award, and has co-authored papers that received the 2010 ISSCC Jack Raper Award for Outstanding Technology Directions Paper, the 2011 Symposium on VLSI Circuits Best Student Paper Award, and the 2012 CICC Best Student Paper Award.

T7: Self-Adapting Design Techniques for Power-Constrained Processors

In today's power-constrained processor designs, self-adaptive design techniques are essential to maximize the performance of a processor under growing variations in process, supply noise, clock skew, and activity. In addition, adaptive designs can reduce design-margin requirements and improve performance by avoiding the over-design that results from metric-based worst-case design methodologies. This tutorial overviews recent techniques for self-adapting design, from industry and academia. Emphasis is placed on various dynamic voltage- and frequency-scaling techniques that adapt to changes in supply noise and processor activities. It then discusses novel methods to improve yield by mitigating design guard-band. The presentation reviews state-of-the-art circuit components necessary to implement these adaptive techniques.

Instructor: Jinuk Luke Shin

Jinuk Luke Shin has been with Oracle (formerly Sun Microsystems) since 2000. He is currently a Director of Hardware Development, responsible for circuit and physical design of next-generation SPARC processors. He has led design activities in technology, power distribution/management, clocking, memories, analog components, Si validation and chip integration for 8 SPARC processors. He received his M.S. degree from the University of Texas at Austin in 1995. Prior to joining Oracle, he was with Motorola, Austin from 1995 to 1997, where he was involved in the design of embedded flash memories for digital signal processors. From 1997 to 2000, he was with Hitachi Semiconductor America, San Jose, CA. His current research interest is in energy-efficient circuit and physical-design techniques and methodologies for high-end microprocessors. He is an author of 35 technical papers and holds 12 issued and pending U.S. patents. He serves as a member of the High-Performance Digital subcommittee of ISSCC.

T8: Interference-Robust CMOS Radio-Receiver Techniques

The radio spectrum is becoming more and more crowded, and radio receivers become interference-limited. As there is a demand for multimode flexible radio devices, traditional dedicated narrowband filtering no longer works. During the last decade, several new radio receiver architectures have been proposed that offer more flexibility than traditional receivers with dedicated fixed filtering, while maintaining good sensitivity and robustness to interference. Different names have been used to refer to these receivers: reconfigurable receiver, multiband receiver, wideband receiver, SAW-less receiver, software-defined radio receiver, or cognitive-radio receiver. These receivers all aim for a high dynamic range while relying less on fixed filters. This tutorial reviews several concepts, including: linearization techniques, noise and distortion cancelling, LNTAs followed by current-mode mixing, mixer-first receivers, frequency-translated filtering, harmonic rejection, and spatial interference rejection.

Instructor: Eric Klumperink

Eric Klumperink received his Ph.D. from Twente University in Enschede in 1997, where he is currently an Associate Professor, teaching Analog and RF CMOS IC Design. His research focus is on Cognitive Radio, Software-Defined Radio and Beamforming. Eric serves as Associate Editor for the Journal of Solid-State Circuits and is a TPC member of ISSCC and RFIC. He holds several patents, has authored or co-authored more than 180 international refereed journal and conference papers, and is a co-recipient of the ISSCC 2002 and the ISSCC 2009 Jan Van Vessem Outstanding Paper Award.

T9: Charge Pump and Capacitive DC-DC Converter Design

Capacitive charge pumps are gaining popularity due to their ease of integration and low EM radiation. Recent research and advances in process technology enable highly efficient, fully integrated DC-DC converters. After an overview of the application field for charge pumps, the tutorial overviews basic structures: the Dickson QP, the basic voltage doubler and the ladder converter, discussing their functionality and their components. Step-up and step-down converters are presented together with techniques to generate different voltage ratios. Advanced topics include ripple reduction by multiphase charge pumps, load and line regulation, control-loop design and design methodologies for optimal efficiency including reducing the influence of device parasitics.

Author: Tim Piessens

Tim Piessens received a Ph.D. degree in 2003 from the University of Leuven. From 1998 to 2003, he was a research assistant at the ESAT-MICAS laboratories under the supervision of Prof. Steyaert. His main research focus was on nonlinear system design and more specific line drivers for xDSL applications. In 2004, Tim cofounded ICsense as a spin-off of the University of Leuven. He works as CTO in the company, with a strong focus on analog and high-voltage IC design. He has authored several ISSCC and JSSC papers and holds several patents.

Presenter: Anton Bakker

Anton Bakker received M.Sc and Ph.D degrees in EE from Delft University in 1991 and 2000 resp. He is the (co)author of over 25 scientific publications and holds 15 patents. From 1991-2000 he was an Assistant Professor at Delft University and since then he has worked for many companies in the Power Management Field including NXP, ADI and MPS. In 2011 he returned to his Alma Mater to teach a course on Power Conversion. He is currently with IDT where he is leading a product development team in the field of Wireless Charging. He has been an ISSCC Analog Subcommittee team member since 2013.

T10: Design of Physical-to-Digital Converters

Modern electronic systems employ increasing numbers of sensors to gather information about the physical world around us. This information, which is inherently non-electrical and analog in nature, needs to be digitized, often with increasingly demanding requirements on accuracy and power efficiency. This tutorial presents an integral approach to designing suitable physical-to-digital converters that goes beyond the conventional approach of combining a sensor, front-end circuit and ADC in terms of accuracy and efficiency. Approaches for embedding sensors into data-converter architectures are presented, including ratiometric charge-balancing architectures and architectures that exploit feedback around the sensor. The need for suitable references and approaches for calibration and correction for cross-sensitivity are addressed. These concepts are illustrated using case studies of state-of-the-art temperature-to-digital, humidity-to-digital, flow-to-digital and light-intensity-to-digital converters.

Instructor: Michiel Pertijs

Michiel Pertijs is an Associate Professor at Delft University of Technology, where he heads a research group working on low-power integrated circuits for medical ultrasound and energy-efficient smart sensors. Prior to this, he was with imec / Holst Centre, and with National Semiconductor, where he designed precision operational amplifiers and instrumentation amplifiers. He has authored or co-authored one book, three book chapters, 11 patents, and over 50 technical papers. He is a program committee member of ISSCC, ESSCIRC, and the IEEE Sensors Conference. He received the ISSCC 2005 Jack Kilby Award and the JSSC 2005 Best Paper Award.

F1: Digitally Assisted Analog and Analog-Assisted Digital in High-Performance Scaled CMOS Process

Organizer: ***Xicheng Jiang,*** *Broadcom, Irvine, CA*

Committee:

Xicheng Jiang, *Broadcom, Irvine, CA*
Piero Malcovati, *University of Pavia, Pavia, Italy*
Vladimir Stojanovic, *MIT, Cambridge, MA*
Iizuka, Tetsuya, *University of Tokyo, Tokyo, Japan*

Digitally assisted analog and analog-assisted digital techniques are increasingly needed in future circuit and system designs, as FinFET and FD-SOI replace planar CMOS technology at the advanced process nodes of 20nm and beyond. The intrinsic features of these new devices are lowering the barrier between the analog and the digital worlds, allowing unprecedented performance to be achieved by assisting digital circuits with analog techniques (e.g. body bias) or by assisting analog circuits with digital techniques (e.g. calibration and run-time control). The objective of the forum is to discuss practical design considerations in high-performance scaled CMOS processes, established circuit techniques that take advantage of scaled CMOS process technology in analog, digital, RF and SoC designs, and an outlook for the future in the context of challenges and solutions.

The forum covers, on one hand, advances in technology, by introducing features and challenges of FinFET and FD-SOI devices and comparing their performance, while, on the other hand, it discusses advances in both analog and digital design enabled by scaled process technologies, in different application fields, ranging from RF to data converters, microprocessors, and mobile SoC.

Agenda

Time	Topic
8:00	Breakfast
8:20	Introduction by the Chair
8:30	**FDSOI Technology for High-Performance and Low-Power Circuit Design,** ***Nicolas Planes,*** *STMicroelectronics, Crolles, France*
9:20	**FinFET Technology for High-Performance Circuit Design**, ***Tatsuya Ohguro,*** *Toshiba, Yokohama, Japan*
10:10	Break
10:35	**Digitally Assisted Analog Design Enables Mobile SoC Evolution,** ***Todd Brooks****, Broadcom, Irvine, CA*
11:25	**Analog-Assisted Digital Design in Mobile SoCs**, ***Martin Saint-Laurent,*** *Qualcomm, Austin, TX*
12:15	Lunch
13:20	**Charge-Steering Techniques for Gigahertz Analog and Digital Circuits**, ***Behzad Razavi,*** *University of California, Los Angeles, CA*
14:10:	**Digitally Assisted Data Converter Techniques,** ***Ian Galton,*** *University of California, San Diego, CA*
15:00:	Break
15:20	**Digitally Intensive CMOS Transmitters**, ***Mark Ingels,*** *imec, Leuven, Belgium*
16:10	**Multi-band Radios in Deep-Scaled CMOS by Using On-Chip Self-Healing Algorithm and Digitally Controlled Artificial Dielectric**, ***Frank Chang,*** *University of California, Los Angeles, CA*
17:00	Closing Remarks

F2: 3D Stacking Technologies for Image Sensors and Memories

Organizer: ***Yusuke Oike,*** *Sony, Kanagawa, Japan*

Committee:

Yusuke Oike, *Sony, Kanagawa, Japan*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Albert Theuwissen, *Harvest Imaging and TU Delft, Delft, Belgium*
Johannes Solhusvik, *Omnivision, Oslo, Norway*
Jonathan Chang, *TSMC, Hsinchu, Taiwan*
Tadahiro Kuroda, *Keio University, Kanagawa, Japan*

Three-dimensional (3D) stacking integration is offering many product benefits to SoC and memory: performance enhancements, product miniaturization and cost reduction. Besides image sensors featuring 3D stacking of a specialized image sensor layer on the top of a deep submicron digital CMOS have just come to the market. The objective of this forum is to present applications and details of process integration, device techniques, circuits and system featuring 3D stacking integration. This will start with an overview of 3D stacking ICs, followed by a system perspective with scaling the memory wall. The next two talks will discuss challenges for power reduction with wide memory bandwidth, and performance gains through advanced packaging and chip stacking. This is followed by two talks covering challenges for foundry-specific issues and impact on device performance. The last two talks highlight how to integrate an imaging device on an SoC layer: technical issues and phenomenon of 3D stacked image sensor products, and evolution of 3D integration for imaging system.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Yusuke Oike,** *Sony, Kanagawa, Japan*
08:30	**3D System Module with Stacked Image Sensors, Stacked Memories and Stacked Processors on a Si Interposer** ***Mitsumasa Koyanagi ,*** *Tohoku University, Sendai, Japan*
09:20	**Scaling the Memory Wall with 3D-IC: A System Perspective** ***Shih-Lien Lu,*** *Intel, Hillsboro, Oregon*
10:10	Break
10:35	**3D-TSV Integration of Memory and SoC for Low Power Applications** ***Ho-Kyu Kang,*** *Samsung Electronics, Hwasung, Korea*
11:25	**Orthogonal Scaling - the Role of Packaging and 3D Integration** ***Subramanian Iyer,*** *IBM, Hopewell Junction, New York*
12:15	Lunch
13:20	**Challenges and Opportunities of 3D Chips Stacking - A Foundry's Perspective** ***Douglas Yu,*** *TSMC, Hsinchu, Taiwan*
14:10	**3D System Integration – Mitigating the Impact on CMOS Device Performance** ***Eric Beyne,*** *imec, Leuven, Belgium*
15:00	Break
15:20	**3D Stacked CMOS Image Sensor Exmor RS™** ***Taku Umebayashi,*** *Sony, Kanagawa, Japan*
16:10	**Evolution of 3D Integration for CMOS Image Sensor Cameras** ***Lindsay Grant,*** *STMicroelectronics, Edinburgh, United Kingdom*
17:30	Closing Remarks (Chair)

ES1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 23 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three sessions: Data Converters and RF/MMICs; Circuits and Systems for Bio-medical Applications and Analog Techniques; Digital, Imagers, and Si Photonics.

The Student Research Preview will begin with a brief talk by a Distinguished member of the solid-state circuit community, Professor Asad Abidi of UCLA. He will reveal a modern quantified understanding of the regenerative latch, an increasingly critical element in the analog-to-digital interface. These remarks are scheduled for Sunday, February 9th, starting at 7:30 pm. SRP is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel**	University of Pennsylvania, USA
Co-Chair:	**SeongHwan Cho**	KAIST, Korea
Co-Chair:	**Marian Verhelst**	Kath. University of Leuven, Belgium
Secretary:	**Tsung-Hsien Lin**	National Taiwan University, Taiwan
Advisor:	**Kenneth C. Smith**	University of Toronto, Canada
Media/Publications:	**Laura Fujino**	University of Toronto, Canada
A/V:	**John Trnka**	Rochester, MN

Committee Members

Bryan Ackland	Stevens Institute of Technology, USA
Bevan Baas	University of California, Davis, USA
Andrea Baschirotto	University of Milan-Bicocca, Italy
Jean-Baptiste Begueret	IMS Labs, France
William Bowhill	Intel, USA
Brian Lum Shue Chan	Texas Instruments, USA
SeongHwan Cho	KAIST, Korea
Denis Daly	Maxim Integrated, USA
Andreas Demosthenous	University College London, UK
Vincent Gaudet	University of Waterloo, Canada
Makoto Ikeda	University of Tokyo, Japan
Takayuki Kawahara	Hitachi, Japan
Jaeha Kim	Seoul National University, Korea
Tsung-Hsien Lin	National Taiwan University, Taiwan
Shen-Iuan Liu	National Taiwan University, Taiwan
Dejan Markovic'	University of California, Los Angeles, USA
Akira Matsuzawa	Tokyo Institute of Technology, Japan
Shahriar Mirabbasi	University of British Columbia, Canada
Tinoosh Mohsenin	Univ. of Maryland, USA
Kostas Pagiamtzis	Semtech, Canada
Patrick Reynaert	K.U. Leuven, Belgium
Bing Sheu	TSMC
Sameer Sonkusale	Tufts University, USA
Jan Van der Spiegel	University of Pennsylvania, USA
Marian Verhelst	Kath. University of Leuven, Belgium
Zhihua Wang	Tsinghua University, P.R. China
Jeff Weldon	Carnegie Mellon University, USA

ES2: Data Centers to Support Tomorrow's Cloud

Organizers: **Leland Chang,** *IBM, Yorktown Heights, NY*
Ajith Amerasekera, *Texas Instruments, Dallas, TX*
Takashi Hashimoto, *Panasonic, Fukuoka City, Fukuoka, Japan*

Chair: **Leland Chang,** *IBM, Yorktown Heights, NY*

With the rise of cloud computing and Big Data, data centers are an important counterpoint to rapid growth in the mobile market. Building cost-effective, efficient computing infrastructures is a challenge that starts with technologies that ISSCC knows so well (processors, I/O, memory, etc.), but also encompasses system and customer-centric issues such as cooling, power delivery, and total cost of ownership. An outlook on the future of data centers will be discussed, including recent trends such as open source models, energy-proportional computing, disaggregation, and software-defined data centers will be discussed as they pertain to the ISSCC community.

Time	Topic
8:00	**Today's Big (data) Is Small** **Steve Pawlowski,** *Intel, Hillsboro, OR*
8:30	**Healthcare in the Big Data Era** **Yasunori Kimura,** *Fujitsu, Sunnyvale, CA*
9:00	**Evolution of ARM Technology Towards the Data Center** **John Goodacre,** *ARM, United Kingdom*
9:30	**Landheld Computing** **Luiz André Barroso,** *Google, Mountain View, CA*
10:05	**Conclusion**

Plenary Session — Invited Papers

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair:
Trudy Stetzler, *Halliburton Houston, TX*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE ***8:30AM***

8:45AM

1.1 Computing's Energy Problem (and what we can do about it)

Mark Horowitz, *Yahoo! Founder's Chair, Stanford University, Stanford, CA, USA*

Almost all electronic systems are energy-limited, from the computers in your Bluetooth headset, to the ones that answer the questions that you type into Google. Performance optimization drove us to this energy limit, even before the energy scaling of gates slowed down. Now that gate energy is scaling slowly, the problem is even worse. While previous energy limits were overcome by changing technology (tubes, transistors, CMOS) I will explain why we can not count on technology saving the day this time.

We next look at making a modern web-server farm more efficient. As CPUs have improved, memory and I/O-system energy dominate. While reducing this energy is possible, this fact raises the question of how ASICs can be 1000× more efficient than processors, if memory energy dominates. Their secret lies in the ASIC's choice of applications: those that have many short-integer operations and extremely local storage. The rest of the presentation will explain how we have leveraged this insight, both to create a programmable unit with ASIC efficiencies, and to bound the amount of compute specialization needed to create energy-efficient hardware for other classes of applications.

9:20AM

1.2: Cloud 2.0 Clients and Connectivity – Technology and Challenges

Ming-Kai Tsai, *Chairman and CEO, MediaTek, Hsinchu, Taiwan*

Two key enablers for distributed web services, or Cloud 1.0, are clients such as smartphones and tablets, and connectivity. To satisfy growing computing requirements, mobile CPU clock frequencies have exceeded GHz. However, the technology will soon hit a frequency wall beyond which cost becomes prohibitively high. Thus, mobile clients are rapidly moving to multi-core CPU and GPU structures to enable consumer applications and mobile human-interface devices (HIDs), with system-adaptive power management, thermal throttling, and heterogeneous multi-processing, for optimal performance and energy efficiency within thermal limits. On the other hand, while wired communication, LAN, and WAN, all drove Cloud 1.0, it is wireless WAN technology that enabled users to stay connected anywhere at anytime. Soon, Cloud 1.0 will morph into Cloud 2.0, heralding the ubiquitous era where the central cloud will be distributed into personal (e.g., Smartphone, Tablet), home (e.g., Smart-TV), and local clouds. The insatiable computation need, coupled with the explosion of Internet-of-Things (IoT) devices and distributed clouds, demands orders-of-magnitude higher bandwidth for better user experience. But, with the constraints of portable-device form factor and limited battery-technology improvement, the energy and thermal gaps present major technical challenges. To overcome these challenges, many innovations are desperately needed to enable the ubiquitous Cloud 2.0 ecosystem which promises to provide ample possibilities to enhance and enrich everyone's life.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS *9:55AM*

BREAK *10:25AM*

1.3 How Chips Pave the Road to the Higgs Particle and the Attoworld Beyond DS *10:40AM*

Erik H.M. Heijne, *Instrumentation Physicist, CERN PH Department, Geneva, Switzerland, also with IEAP Czech Technical University Prague & Nikhef Amsterdam*

Fundamental research on elementary constituents of matter needs ever-higher energies, and sophisticated instrumentation. Segmented low capacitance silicon PIN diode sensors and CMOS circuits have proved essential to the recent discovery of the Higgs boson at the CERN Large Hadron Collider (LHC). Custom ICs provided a paradigm shift in experimental techniques, permitting event imaging and selection at unprecedented rates. Four experiments at the Collider act as giant cameras, each taking 40 million 3D pictures per second. In the largest experiment six concentric subsystems with ~500 million sensor elements allow precise localization of thousands of particles per collision. The readout chips need adequate timing, noise, power and matching performance and must be radiation tolerant. The Worldwide LHC Computing Grid (WLCG) enabled quick analysis of the massive data volume. This presentation describes how custom VLSI chips combined with silicon detectors contribute to our understanding of Nature.

1.4: The Next Generation of Networked Experiences *11:15AM*

Susie Wee, *Vice President & Chief Technology Officer of Networked Experiences, Cisco, San Jose, CA*

The evolution of network technology has enabled impressive networked experiences, ranging from connected mobile context-aware experiences to those provided by large-screen interactive immersive video dislays. The rapid pace of innovation and the trends in consumerization have made these experiences affordable and widely available, greatly increasing end users' expectations. In the years ahead, networks will undergo the greatest architectural transition seen in the past two decades, with the advent of software-defined networks, big data, and the internet of things. By taking an experience-driven approach to this architectural shift, we can understand the network and technology requirements for the underlying compute and network infrastructure, client devices, and sensors and the interaction of applications with the network. In this presentation, I will discuss the next generation of networked experiences and the technology innovations that will be needed in the years to come.

PRESENTATION TO PLENARY SPEAKERS *11:50AM*

CONCLUSION *11:55AM*

Ultra-High-Speed Wireline Transceivers and Techniques

Session Chair: Ken Chang, *Xilinx, San Jose, CA*
Associate Chair: Koichi Yamaguchi, *Renesas Electronics, Kawasaki, Japan*

2.1 28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28nm CMOS (DS) **1:30 PM**
H. Kimura, P. Aziz, T. Jing, A. Sinha, R. Narayan, H. Gao, P. Jing, G. Hom, A. Liang, E. Zhang, A. Kadkol, R. Kothari, G. Chan, Y. Sun, B. Ge, J. Zeng, K. Ling, M. Wang, A. Malipatil, S. Kotagiri, L. Li, C. Abel, F. Zhong
LSI, San Jose, CA

2.2 A 780mW 4×28Gb/s Transceiver for 100GbE Gearbox PHY in 40nm CMOS **2:00 PM**
U. Singh, A. Garg, B. Raghavan, N. Huang, H. Zhang, Z. Huang, A. Momtaz, J. Cao
Broadcom, Irvine, CA

2.3 60Gb/s NRZ and PAM4 Transmitters for 400GbE in 65nm CMOS **2:30 PM**
P-C. Chiang[1,2], H-W. Hung[1], H-Y. Chu[1], G-S. Chen[1], J. Lee[1,2]
[1]National Taiwan University, Taipei, Taiwan
[2]Atilia Technology, Taipei, Taiwan

Break **3:00 PM**

2.4 A 25Gb/s 5.8mW CMOS Equalizer **3:15 PM**
J. W. Jung, B. Razavi
University of California, Los Angeles, CA

2.5 A 0.25pJ/b 0.7V 16Gb/s 3-Tap Decision-Feedback Equalizer in 65nm CMOS **3:45 PM**
R. Bai[1], S. Palermo[2], P. Y. Chiang[1,3]
[1]Oregon State University, Corvallis, OR; [2]Texas A&M University, College Station, TX
[3]Fudan University, Shanghai, China

2.6 A 5.67mW 9Gb/s DLL-Based Reference-less CDR with Pattern-Dependent Clock-Embedded Signaling for Intra-Panel Interface **4:15 PM**
D. H. Baek[1,2], B. Kim[1], H-J. Park[1], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Yongin, Korea

2.7 A Coefficient-Error-Robust FFE TX with 230% Eye-Variation Improvement Without Calibration in 65nm CMOS Technology **4:30 PM**
S. Han, S. Lee, M. Choi, J-Y. Sim, H-J. Park, B. Kim
Pohang University of Science and Technology, Pohang, Korea

2.8 A Pulse-Position-Modulation Phase-Noise-Reduction Technique for a 2-to-16GHz Injection-Locked Ring Oscillator in 20nm CMOS **4:45 PM**
J-C. Chien[1], P. Upadhyaya[2], H. Jung[2], S. Chen[2], W. Fang[2], A. M. Niknejad[1], J. Savoj[2], K. Chang[2]
[1]University of California, Berkeley, CA
[2]Xilinx, San Jose, CA

2.9 A Background Calibration Technique to Control Bandwidth in Digital PLLs **5:00 PM**
G. Marzin, S. Levantino, C. Samori, A. L. Lacaita
Politecnico di Milano, Milan, Italy

Conclusion **5:15 PM**

RF Techniques

Session Chair: Masoud Zargari, *Qualcomm-Atheros, Irvine, CA*
Associate Chair: Tae Wook Kim, *Yonsei University, Seoul, Korea*

3.1 Polar Antenna Impedance Detection and Tuning for Efficiency Improvement in a 3G/4G CMOS Power Amplifier — **1:30 PM**
S. Kousai, K. Onizuka, T. Yamaguchi, Y. Kuriyama, M. Nagaoka
Toshiba, Kawasaki, Japan

3.2 A 1.95GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier with Envelope/Phase Generator and Timing Aligner for WCDMA and LTE — **2:00 PM**
K. Oishi[1], E. Yoshida[1], Y. Sakai[1], H. Takauchi[1], Y. Kawano[1], N. Shirai[2], H. Kano[2], M. Kudo[2], T. Murakami[2], T. Tamura[2], S. Kawai[2], S. Yamaura[2], K. Suto[2], H. Yamazaki[1], T. Mori[1]
[1]Fujitsu Laboratories, Kawasaki, Japan
[2]Fujitsu Semiconductor, Yokohama, Japan

3.3 A Transformer-Coupled True-RMS Power Detector in 40nm CMOS — **2:30 PM**
B. Francois, P. Reynaert, KU Leuven, Leuven, Belgium

3.4 A Dual-Mode Transformer-Based Doherty LTE Power Amplifier in 40nm CMOS — **2:45 PM**
E. Kaymaksut, P. Reynaert, KU Leuven, Leuven, Belgium

Break — **3:00 PM**

3.5 A 1.0-to-2.5GHz Beamforming Receiver with Constant-G_m Vector Modulator Consuming < 9mW per Antenna Element in 65nm CMOS — **3:15 PM**
M. C. Soer[1], E. A. Klumperink[1], B. Nauta[1], F. E. van Vliet[1,2]
[1]University of Twente, Enschede, The Netherlands
[2]TNO Science and Industry, The Hague, The Netherlands

3.6 A Noise-Cancelling Receiver with Enhanced Resilience to Harmonic Blockers — **3:30 PM**
D. Murphy, H. Darabi, H. Xu, Broadcom, Irvine, CA

3.7 A Fully Integrated TV Tuner Front-End with 3.1dB NF, >+31dBm OIP3, >83dB HRR3/5 and >68dB HRR7 — **3:45 PM**
I-Y. Lee[1], S-S. Lee[1], D. Im[2], S. Kim[1], J. Choi[3], S-G. Lee[1], J. Ko[3]
[1]KAIST, Daejeon, Korea
[2]University of Texas, Dallas, Richardson, TX
[3]PHYCHIPS, Daejeon, Korea

3.8 A Fully Integrated Highly Reconfigurable Discrete-Time Super-Heterodyne Receiver — **4:15 PM**
M. Tohidian, I. Madadi, R. B. Staszewski
Delft University of Technology, Delft, The Netherlands

3.9 An RF-to-BB Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF — **4:45 PM**
F. Lin[1], P-I. Mak[1,2], R. Martins[1,2,3]
[1]University of Macau, Macao, China
[2]UMTEC, Macao, China
[3]Instituto Superior Tecnico, Lisbon, Portugal

Conclusion — **5:00 PM**

DC-DC Converters

Session Chair: Wing-Hung Ki, *Hong Kong University of Science and Technology, Hong Kong, Hong Kong*
Associate Chair: Christoph Sandner, *Infineon Technologies, Villach, Austria*

4.1 A 3-Phase Digitally Controlled DC-DC Converter with 88% Ripple Reduced 1-Cycle Phase Adding/Dropping Scheme and 28% Power Saving CT/DT Hybrid Current Control — 1:30 PM
C. K. Teh, A. Suzuki, M. Yamada, M. Hamada, Y. Unekawa
Toshiba, Kawasaki, Japan

4.2 A 6A 40MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient — 2:00 PM
M. K. Song, J. Sankman, D. Ma
University of Texas, Dallas, Richardson, TX

4.3 An 87%-Peak-Efficiency DVS-Capable Single-Inductor 4-Output DC-DC Buck Converter with Ripple-Based Adaptive Off-Time Control — 2:30 PM
D. Lu, Y. Qian, Z. Hong
Fudan University, Shanghai, China

Break — 3:00 PM

4.4 A 10/30MHz Wide-Duty-Cycle-Range Buck Converter with DDA-Based Type-III Compensator and Fast Reference-Tracking Responses for DVS Applications — 3:15 PM
L. Cheng, Y. Liu, W-H. Ki
Hong Kong University of Science and Technology, Hong Kong, China

4.5 A 2-Phase Resonant Switched-Capacitor Converter Delivering 4.3W at 0.6W/mm² with over 85% Efficiency — 3:45 PM
K. Kesarwani, R. Sangwan, J. T. Stauth
Dartmouth College, Hanover, NH

4.6 An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range — 4:15 PM
L. G. Salem, P. P. Mercier
University of California, San Diego, La Jolla, CA

4.7 A Sub-ns Response On-Chip Switched-Capacitor DC-DC Voltage Regulator Delivering 3.7W/mm² at 90% Efficiency Using Deep-Trench Capacitors in 32nm SOI CMOS — 4:45 PM
T. M. Andersen[1,2], F. Krismer[1], J. W. Kolar[1], T. Toif[2], C. Menolfi[2], L. Kull[2], T. Morf[2], M. Kossel[2], M. Brändli[2], P. Buchmann[2], P. A. Francese[2]
[1]ETH, Zurich, Switzerland
[2]IBM Research, Rüschlikon, Switzerland

4.8 3-Phase 6/1 Switched-Capacitor DC-DC Boost Converter Providing 16V at 7mA and 70.3% Efficiency in 1.1mm³ — 5:00 PM
R. Karadi, G. Villar Pique
NXP Semiconductors, Eindhoven, The Netherlands

Conclusion — 5:15 PM

Processors

Session Chair: Atsuki Inoue, *Fujitsu, Kawasaki, Japan*
Associate Chair: Christopher Gonzalez, *IBM, Poughkeepsie, NY*

5.1 POWER8™: A 12-Core Server-Class Processor in 22nm SOI with 7.6Tb/s Off-Chip Bandwidth — **1:30 PM**
E. J. Fluhr[1], J. Friedrich[1], D. Dreps[1], V. Zyuban[2], G. Still[3], C. Gonzales[4], A. Hall[1], D. Hogenmiller[1], F. Malgioglio[4], R. Nett[1], J. Paredes[1], J. Pille[3], D. Plass[4], R. Puri[2], P. Restle[2], D. Shan[1], K. Stawiasz[2], Z. T. Deniz[2], D. Wendel[5], M. Ziegler[2]
[1]IBM STG, Austin, TX; [2]IBM T. J. Watson, Yorktown Heights, NY
[3]IBM STG, Raleigh, NC; [4]IBM STG, Poughkeepsie, NY
[5]IBM STG, Boeblingen, Germany

5.2 Distributed System of Digitally Controlled Microregulators Enabling Per-Core DVFS for the POWER8™ Microprocessor — **2:00 PM**
Z. Toprak-Deniz[1], M. Sperling[2], J. Bulzacchelli[1], G. Still[3], R. Kruse[4], S. Kim[1], D. Boerstler[4], T. Gloekler[5], R. Robertazzi[1], K. Stawiasz[1], T. Diemoz[2], G. English[2], D. Hui[2], P. Muench[2], J. Friedrich[4]
[1]IBM, Yorktown Heights, NY; [2]IBM, Poughkeepsie, NY; [3]IBM, Raleigh, NC
[4]IBM, Austin, TX; [5]IBM, Boeblingen, Germany

5.3 Wide-Frequency-Range Resonant Clock with On-the-Fly Mode Changing for the POWER8™ Microprocessor — **2:15 PM**
P. Restle[1], D. Shan[2], D. Hogenmiller[2], Y. Kim[2], A. Drake[3], J. Hibbeler[4], T. Bucelot[1], G. Still[5], K. Jenkins[1], J. Friedrich[2]
[1]IBM Research, Yorktown Heights, NY; [2]IBM STG, Austin, TX
[3]IBM Research, Austin, TX; [4]IBM STG, Williston, VT; [5]IBM STG, Raleigh, NC

5.4 Ivytown: A 22nm 15-Core Enterprise Xeon® Processor Family — DS — **2:30 PM**
S. Rusu, H. Muljono, D. Ayers, S. Tam, W. Chen, A. Martin, S. Li, S. Vora, R. Varada, E. Wang
Intel, Santa Clara, CA

Break — **3:00 PM**

5.5 Steamroller: An x86-64 Core Implemented in 28nm Bulk CMOS — **3:15 PM**
K. Gillespie[1], H. R. Fair III[1], C. Henrion[2], R. Jotwani[3], S. Kosonocky[2], R. S. Orefice[1], D. A. Priore[1], J. White[1], K. Wilcox[1]
[1]AMD, Boxborough, MA; [2]AMD, Fort Collins, CO; [3]AMD, Austin, TX

5.6 Adaptive Clocking System for Improved Power Efficiency in a 28nm x86-64 Microprocessor — **3:45 PM**
A. Grenat[1], S. Pant[1], R. Rachala[1], S. Naffziger[2]
[1]AMD, Austin, TX; [2]AMD, Fort Collins, CO

5.7 A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep — DS — **4:00 PM**
C. Tokunaga, J. F. Ryan, C. Augustine, J. P. Kulkarni, Y-C. Shih, S. T. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. M. Khellah, J. W. Tschanz, V. De
Intel, Hillsboro, OR

5.8 A 3GHz 64b ARM v8 Processor in 40nm Bulk CMOS Technology — **4:15 PM**
A. Yeung, H. Partovi, Q. Harvard, L. Ravezzi, J. Ngai, R. Homer, M. Ashcraft, G. Favor
Applied Micro, Sunnyvale, CA

5.9 Haswell: A Family of IA 22nm Processors — DS — **4:45 PM**
N. Kurd, M. Chowdhury, E. Burton, T. P. Thomas, C. Mozak, B. Boswell, M. Lal, A. Deval, J. Douglas, M. Elassal, A. Nalamalpu, T. M. Wilson, M. Merten, S. Chennupaty, W. Gomes, R. Kumar
Intel, Hillsboro, OR

Conclusion — **5:15 PM**

Technologies for High-Speed Data Networks

Session Chair: Pirooz Parvarandeh, *Maxim Integrated, San Jose, CA*
Associate Chair: Chris Nicol, *Wave Semiconductor, Sunnyvale, CA*

6.1 Memory and System Architecture for 400Gb/s Networking and Beyond — **1:30 PM**
D. Maheshwari
Cypress Semiconductor, San Jose, CA

6.2 High-Capacity Scalable Optical Communication for Future Optical Transport Network — **2:00 PM**
Y. Miyamoto, M. Tomizawa
NTT, Yokosuka, Japan

6.3 A Heterogeneous 3D-IC Consisting of Two 28nm FPGA Die and 32 Reconfigurable High-Performance Data Converters — **2:30 PM**
C. Erdmann[1], D. Lowney[1], A. Lynam[1], A. Keady[1], J. McGrath[1], E. Cullen[1], D. Breathnach[1], D. Keane[1], P. Lynch[1], M. De La Torre[1], R. De La Torre[1], P. Lim[1], A. Collins[1], B. Farley[1], L. Madden[2]
[1]Xilinx, Dublin, Ireland
[2]Xilinx, San Jose, CA

Break — **3:00 PM**

Image Sensors

Session Chair: Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Associate Chair: David Stoppa, *Fondazione Bruno Kessler, Trento, Italy*

7.1 A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12μm Pixel with Front-Side Deep-Trench Isolation and Vertical Transfer Gate **3:15 PM**
J. Ahn, K. Lee, Y. Kim, H. Jeong, B. Kim, H. Kim, J. Park, T. Jung, W. Park, T. Lee, E. Park, S. Choi, G. Choi, H. Park, Y. Choi, S. Lee, Y. Kim, Y. J. Jung, D. Park, S. Nah, Y. Oh, M. Kim, Y. Lee, Y. Chung, I. Hisanori, J. Im, D-K. Lee, B. Yim, G. Lee, H. Kown, S. Choi, J. Lee, D. Jang, Y. Kim, T. C. Kim, G. Hiroshige, C-Y. Choi, D. Lee, G. Han
Samsung Electronics, Yongin, Korea

7.2 243.3pJ/pixel Bio-Inspired Time-Stamp-Based 2D Optic Flow Sensor for Artificial Compound Eyes **3:45 PM**
S. Park, J. Cho, K. Lee, E. Yoon
University of Michigan, Ann Arbor, MI

7.3 A 1000fps Vision Chip Based on a Dynamically Reconfigurable Hybrid Architecture Comprising a PE Array and Self-Organizing Map Neural Network **4:00 PM**
C. Shi[1,2], J. Yang[1], Y. Han[1], Z. Cao[1], Q. Qin[1], L. Liu[1], N-J. Wu[1], Z. Wang[2]
[1]Chinese Academy of Sciences, Beijing, China
[2]Tsinghua University, Beijing, China

7.4 A 413×240-Pixel Sub-Centimeter Resolution Time-of-Flight CMOS Image Sensor with In-Pixel Background Canceling Using Lateral-Electric-Field Charge Modulators **4:15 PM**
S-M. Han[1], T. Takasawa[1], T. Akahori[2], K. Yasutomi[1], K. Kagawa[1], S. Kawahito[1,2]
[1]Shizuoka University, Hamamatsu, Japan
[2]Brookman Technology, Hamamatsu, Japan

7.5 A 0.3mm-Resolution Time-of-Flight CMOS Range Imager with Column-Gating Clock-Skew Calibration **4:30 PM**
K. Yasutomi, T. Usui, S-M. Han, T. Takasawa, K. Kagawa, S. Kawahito
Shizuoka University, Hamamatsu, Japan

7.6 A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC DS **4:45 PM**
A. Payne, A. Daniel, A. Mehta, B. Thompson, C. S. Bamji, D. Snow, H. Oshima, L. Prather, M. Fenton, L. Kordus, P. O'Connor, R. McCauley, S. Nayak, S. Acharya, S. Mehta, T. Elkhatib, T. Meyer, T. O'Dwyer, T. Perry, V-H. Chan, V. Wong, V. Mogallapu, W. Qian, Z. Xu
Microsoft, Mountain View, CA

Conclusion **5:15 PM**

DEMONSTRATION SESSION (DS)*MONDAY, FEBRUARY 10TH 4:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday, February 10, from 4 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2014, as noted by the symbol DS

Monday February 10th

1.3	How Chips Pave the Road to the Higgs Particle and the Attoworld Beyond	10:40 AM
2.1	28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28nm CMOS	1:30 PM
5.4	Ivytown: A 22nm 15-Core Enterprise Xeon® Processor Family	2:30 PM
5.7	A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep	4:00 PM
5.9	Haswell: A Family of IA 22nm Processors	4:45 PM
7.6	A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC	4:45 PM

Tuesday February 11th

8.2	A 12×5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS	9:00 AM
9.1	A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11μm CMOS	8:30 AM
9.7	A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM-Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications	11:45 AM
10.6	A 0.74V 200μW Multi-Standard Transceiver Digital Baseband in 40nm LP-CMOS for 2.4GHz Bluetooth Smart / ZigBee / IEEE 802.15.6 Personal Area Networks	11:00 AM
10.7	A 105GOPS 36mm^2 Heterogeneous SDR MPSoC with Energy-Aware Dynamic Scheduling and Iterative Detection-Decoding for 4G in 65nm CMOS	11:15 AM
11.3	A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation	9:30 AM
12.1	3D Ultrasonic Gesture Recognition	8:30 AM
12.2	3D Gesture-Sensing System for Interactive Displays Based on Extended-Range Capacitive Sensing	9:00 AM

Tuesday February 11th

12.3	A 240Hz-Reporting-Rate 143×81 Mutual-Capacitance Analog Touch-Sensing Front-End IC with 37dB SNR for 1mm-Diameter Stylus	9:15 AM
12.4	A 1mm-Pitch 80×80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan	9:30 AM
12.8	A BJT-Based CMOS Temperature Sensor with a 3.6pJ·K^2-Resolution FoM	11:30 AM
13.1	A 1Gb 2GHz Embedded DRAM in 22nm Tri-Gate CMOS Technology	1:30 PM
14.5	A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13μm SiGe BiCMOS	3:15 PM
16.1	A 340mV-to-0.9V 20.2Tb/s Source-Synchronous Hybrid Packet/Circuit-Switched 16×16 Network-on-Chip in 22nm Tri-Gate CMOS	3:15 PM
17.4	CMOS Impedance Analyzer for Nanosamples Investigation Operating up to 150MHz with Sub-aF Resolution	2:30 PM
18.1	A 1V 3mA 2.4GHz Wireless Digital Audio Communication SoC for Hearing-Aid Applications in 0.18μm CMOS	1:30 PM
18.2	A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18μm HVCMOS	2:00 PM
18.3	A Multi-Parameter Signal-Acquisition SoC for Connected Personal Health Applications	2:30 PM

Wednesday February 12th

20.5	A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput	10:30 AM
22.5	A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS	10:45 AM
26.2	A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS	3:45 PM
26.3	A Pin- and Power-Efficient Low-Latency 8-to-12Gb/s/wire 8b8w-Coded SerDes Link for High-Loss Channels in 40nm Technology	4:15 PM
30.2	Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption	2:00 PM

EP1: Next-Generation Networked Systems: Challenges for Silicon

Organizer: **Hoi-Jun Yoo,** *KAIST, Daejeon, Korea,*

Moderators: **Anantha Chandrakasan,** *MIT, Cambridge, MA*
Siva Narendra, *Tyfone, Portland, OR*

Semiconductor systems connected through wireless and wired networks are the mainstream approach in the semiconductor market to achieve technical innovations and business advantages. Systems are defined differently according to the application area, implementation technology and also the individual engineer's background. This presents challenges to circuit designers and circuit-design educators.

Does the design primarily belong to system architects or to circuit designers? Is domain-specific knowledge, for example biomedical or automotive, essential for system development? Can the domain expert alone, rather than the system architect, design and develop the system as the principal engineer? Or is it possible for the circuit designer to provide a "system platform" to the domain experts for their applications? Are there any good examples where the semiconductor technology and circuits contribute mainly to the innovation of the total system performance? Are MEMS integration, or integration of a temperature-sensing circuit on an SoC, good examples?

Experts on the system side and the traditional silicon side will share their experiences and vision about the development of innovative systems based on semiconductor technology and circuits.

Panelists:

Alex Jinsung Choi, *SK Telecom, Seoul, Korea*
William Dally, *NVIDIA, Santa Clara, CA*
Robert Gilmore, *Qualcomm, San Diego, CA*
Mike Muller, *ARM, Cambridge, United Kingdom*
Udo-Martin Gomez, *Bosch Sensortec, Stuttgart, Germany*
Atsushi Takahara, *NTT, Yokosuka, Japan*

Optical Links and Copper PHYs

Session Chair: Ichiro Fujimori, *Broadcom, Irvine, CA*
Associate Chair: Hideyuki Nosaka, *NTT, Atsugi, Japan*

8.1 A 6Gb/s Transceiver with a Nonlinear Electronic Dispersion Compensator for Directly Modulated Distributed-Feedback Lasers — **8:30 AM**
K. Kwon, J. Yoon, S-W. Kwon, J. Yang, J-Y. Lee, H. Won, H-M. Bae
KAIST, Daejeon, Korea

8.2 A 12×5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS — DS — **9:00 AM**
H. Morita, K. Uchino, E. Otani, H. Ohtorii, T. Ogura, K. Oniki, S. Oka, S. Yanagawa, H. Suzuki
Sony, Tokyo, Japan

8.3 A Power-Scalable 7-Tap FIR Equalizer with Tunable Active Delay Line for 10-to-25Gb/s Multi-Mode Fiber EDC in 28nm LP-CMOS — **9:30 AM**
E. Mammei[1], F. Loi[1], F. Radice[2], A. Dati[2], M. Bruccoleri[2], M. Bassi[1], A. Mazzanti[1]
[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Cornaredo, Italy

8.4 A 28Gb/s 1pJ/b Shared-Inductor Optical Receiver with 56% Chip-Area Reduction in 28nm CMOS — **9:45 AM**
T-C. Huang[1], T-W. Chung[2], C-H. Chern[1], M-C. Huang[1], C-C. Lin[1], F-L. Hsueh[3]
[1]TSMC Design Technology, San Jose, CA; [2]nVidia, San Jose, CA
[3]TSMC, Hsinchu, Taiwan

Break — **10:00 AM**

8.5 A Sub-1.75W Full-Duplex 10GBASE-T Transceiver in 40nm CMOS — **10:15 AM**
J. R. Westra, J. Mulder, Y. Ke, D. Vecchi, X. Liu, E. Arslan, J. Wan, Q. Zhang, S. Wang, F. M. van der Goes, K. Bult
Broadcom, Bunnik, The Netherlands

8.6 A Full-Duplex Line Driver for Gigabit Ethernet with Rail-to-Rail Class-AB Output Stage in 28nm CMOS — **10:45 AM**
H. Pan, Y. Yao, M. Hammad, J. Tan, K. Abdelhalim, E. Wang, R. Hsu, J. Yu, J. Aziz, D. Tam, I. Fujimori
Broadcom, Irvine, CA

8.7 A 4-to-10.5Gb/s 2.2mW/Gb/s Continuous-Rate Digital CDR with Automatic Frequency Acquisition in 65nm CMOS — **11:15 AM**
G. Shu[1], W.-S. Choi[1], S. Saxena[1], T. Anand[1], A. Elshazly[2], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL
[2]Intel, Hillsboro, OR

8.8 An 8.2-to-10.3Gb/s Full-Rate Linear Reference-less CDR Without Frequency Detector in 0.18μm CMOS — **11:45 AM**
S. Huang[1], J. Cao[2], M. M. Green[1]
[1]University of California, Irvine, CA
[2]Broadcom, Irvine, CA

8.9 A 40Gb/s VCSEL Over-Driving IC with Group-Delay-Tunable Pre-Emphasis for Optical Interconnection — **12:00 PM**
Y. Tsunoda, M. Sugawara, H. Oku, S. Ide, K. Tanaka
Fujitsu Laboratories, Atsugi, Japan

Conclusion — **12:15 PM**

Low-Power Wireless

Session Chair: Jan Crols, *AnSem, Heverlee, Belgium*
Associate Chair: Alyosha Molnar, *Cornell University, Ithaca, NY*

9.1 A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11μm CMOS DS 8:30 AM
W. L. Lien[1], T. Y. Choke[1], Y. C. Tan[1], M. Kong[1], E. C. Low[1], D. P. Li[1], L. Jin[1], H. Zhang[1], C. H. Leow[1], S. L. Chew[1], U. Dasgupta[1], C. H. Yong[1], T. B. Gao[1], G. T. Ong[1], W. G. Tan[1], W. Shu[1], C. L. Heng[1], O. Shana'A[1,2]
[1]MediaTek, Singapore, Singapore; [2]MediaTek, San Jose, CA

9.2 A 13.3mW 500Mb/s IR-UWB Transceiver with Link-Margin Enhancement Technique for Meter-Range Communications 9:00 AM
S. Geng, D. Liu, Y. Li, H. Zhuo, W. Rhee, Z. Wang
Tsinghua University, Beijing, China

9.3 A 1mW 1Mb/s 7.75-to-8.25GHz Chirp-UWB Transceiver with Low Peak Power Transmission and Fast Synchronization Capability 9:30 AM
F. Chen[1], Y. Li[1], D. Liu[1], W. Rhee[1], J. Kim[2], D. Kim[2], Z. Wang[1]
[1]Tsinghua University, Beijing, China
[2]Samsung Advanced Institute of Technology, Suwon, Korea

Break 10:00 AM

9.4 A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components 10:15 AM
Z. Lin[1], P-I. Mak[1,2], R. Martins[1,2,3]
[1]University of Macau, Macao, China; [2]UMTEC, Macao, China
[3]Instituto Superior Tecnico, Lisbon, Portugal

9.5 A 1.2nJ/b 2.4GHz Receiver with a Sliding-IF Phase-to-Digital Converter for Wireless Personal/Body-Area Networks 10:45 AM
Y-H. Liu, A. Ba, J. van den Heuvel, K. Philips, G. Dolmans, H. de Groot
Holst Centre/imec, Eindhoven, The Netherlands

9.6 A 1.3mW 0.6V WBAN-Compatible Sub-Sampling PSK Receiver in 65nm CMOS 11:15 AM
J. Cheng[1], N. Qi[1], P. Y. Chiang[1,2], A. Natarajan[1]
[1]Oregon State University, Corvallis, OR; [2]Fudan University, Shanghai, China

9.7 A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM-Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications DS 11:45 AM
M. Vidojkovic[1], X. Huang[1], X. Wang[1], C. Zhou[1], A. Ba[1], M. Lont[1], Y-H. Liu[1], P. Harpe[2], M. Ding[1], B. Busze[1], N. Kiyani[1], K. Kanda[3], S. Masui[3], K. Philips[1], H. de Groot[1]
[1]Holst Centre/imec, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands
[3]Fujitsu Laboratories, Kawasaki, Japan

9.8 An 860μW 2.1-to-2.7GHz All-Digital PLL-Based Frequency Modulator with a DTC-Assisted Snapshot TDC for WPAN (Bluetooth Smart and ZigBee) Applications 12:00 PM
V. K. Chillara[1,2,], Y-H. Liu[1], B. Wang[1,2], A. Ba[1], M. Vidojkovic[1], K. Philips[1], H. de Groot[1], R. B. Staszewski[2]*
[1]Holst Centre/imec, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
*now with Analog Devices, Limerick, Ireland

Conclusion 12:15 PM

Mobile Systems-on-Chip (SoCs)

Session Chair: Vasantha Erraguntla, *Intel, Bangalore, India*
Associate Chair: Takashi Hashimoto, *Panasonic, Fukuoka, Japan*

10.1 A 28nm DSP Powered by an On-Chip LDO for High-Performance and Energy-Efficient Mobile Applications — 8:30 AM

M. Saint-Laurent[1], P. Bassett[1], K. Lin[2], Y. Wang[2], S. Le[2], X. Chen[2], M. Alradaideh[1], T. Wernimont[1], K. Ayyar[3], D. Bui[1], D. Galbi[1], A. Lester[1], W. Anderson[1]
[1]Qualcomm, Austin, TX; [2]Qualcomm, San Diego, CA; [3]Qualcomm, Bangalore, India

10.2 A 28nm HPM Heterogeneous Multi-Core Mobile Application Processor with 2GHz Cores and Low-Power 1GHz Cores — 9:00 AM

M. Igarashi, T. Uemura, R. Mori, N. Maeda, H. Kishibe, M. Nagayama, M. Taniguchi, K. Wakahara, T. Saito, M. Fujigaya, K. Fukuoka, K. Nii,T. Kataoka, T. Hattori
Renesas Electronics, Tokyo, Japan

10.3 Heterogeneous Multi-Processing Quad-Core CPU and Dual-GPU Design for Optimal Performance, Power, and Thermal Tradeoffs in a 28nm Mobile Application Processor — 9:30 AM

A. Wang[1], T-Y. Lin[2], S. Ouyang[3], W-H. Huang[2], J. Wang[1], S-H. Chang[2], S-P. Chen[2], C-H. Hu[2], J. C. Tai[2], K-S. Tan[2], M-N. Tsou[2], M-H. Lee[2], G. Gammie[1], C-W. Yang[2], C-C. Yang[2], Y-C. Chou[2], S-H. Lin[2], W. Kuo[2], C-J. Chung[2], L-K. Yong[2], C-W. Wang[2], K. H. Dia[2], C-H. Chien[2], Y-M. Tsao[2], N. K. Singh[1], R. Lagerquist[1], C-C. Chen[2], U. Ko[1]
[1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan; [3]MediaTek, San Jose, CA

Break — 10:00 AM

10.4 A 1.22TOPS and 1.52mW/MHz Augmented Reality Multi-Core Processor with Neural Network NoC for HMD Applications — 10:15 AM

G. Kim, Y. Kim, K. Lee, S. Park, I. Hong, K. Bong, D. Shin, S. Choi, J. Oh, H-J. Yoo
KAIST, Daejeon, Korea

10.5 A 90nm 20MHz Fully Nonvolatile Microcontroller for Standby-Power-Critical Applications — 10:45 AM

N. Sakimura[1,2], Y. Tsuji[1], R. Nebashi[1], H. Honjo[1], A. Morioka[1], K. Ishihara[1], K. Kinoshita[2], S. Fukami[2], S. Miura[1], N. Kasai[2], T. Endoh[2], H. Ohno[2], T. Hanyu[2], T. Sugibayashi[1]
[1]NEC, Tsukuba, Japan; [2]Tohoku University, Sendai, Japan

10.6 A 0.74V 200μW Multi-Standard Transceiver Digital Baseband in 40nm LP-CMOS for 2.4GHz Bluetooth Smart / ZigBee / IEEE 802.15.6 Personal Area Networks — DS 11:00 AM

C. Bachmann, G-J. van Schaik, B. Busze, M. Konijnenburg, Y. Zhang, J. Stuyt, M. Ashouei, G. Dolmans, T. Gemmeke, H. de Groot
Holst Centre/imec, Eindhoven, The Netherlands

10.7 A 105GOPS 36mm² Heterogeneous SDR MPSoC with Energy-Aware Dynamic Scheduling and Iterative Detection-Decoding for 4G in 65nm CMOS — DS 11:15 AM

B. Noethen, O. Arnold, E. Perez Adeva, T. Seifert, E. Fischer, S. Kunze, E. Matûs, G. Fettweis, H. Eisenreich, G. Ellguth, S. Hartmann, S. Höppner, S. Schiefer, J-U. Schlüßler, S. Scholze, D. Walter, R. Schüffny
Technische Universität Dresden, Dresden, Germany

10.8 A Multi-Standard 2G/3G/4G Cellular Modem Supporting Carrier Aggregation in 28nm CMOS — 11:45 AM

M. Breschel[1], P. Almers[1], F. Angsmark[1], A. Arvidsson[1], H. Bauer[2], K. van Berkel[3], J. Canovas[1], M. Do[1], A. Ekelund[1], T. Larsson[1], B. Lincoln[1], M. Malmberg[1], M. Naruse[4], M. Onishi[4], C. Östberg[1], J-P. Smeets[3], M. Vergara Escobar[1], J. Voelkl[2], E. Wittenmark[1]
[1]Ericsson, Lund, Sweden; [2]Ericsson, Nuremberg, Germany
[3]Ericsson, Eindhoven, The Netherlands; [4]Ericsson, Yokohama, Japan

Conclusion — 12:15 PM

Data Converter Techniques

Session Chair: Jan Mulder, *Broadcom, Bunnik, The Netherlands*
Associate Chair: Stéphane Le Tual, *STMicroelectronics, Crolles, France*

11.1 An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR — **8:30 AM**
P. Harpe, E. Cantatore, A. van Roermund
Eindhoven University of Technology, Eindhoven, The Netherlands

11.2 A 0.85fJ/conversion-step 10b 200kS/s Subranging SAR ADC in 40nm CMOS — **9:00 AM**
H-Y. Tai, Y-S. Hu, H-W. Chen, H-S. Chen
National Taiwan University, Taipei, Taiwan

11.3 A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation — DS **9:30 AM**
F. M. Yaul, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

Break — **10:00 AM**

11.4 A 1.5mW 68dB SNDR 80MS/s 2× Interleaved SAR-Assisted Pipelined ADC in 28nm CMOS — **10:15 AM**
F. van der Goes[1], C. Ward[1], S. Astgimath[2], H. Yan[1], J. Riley[1], J. Mulder[1], S. Wang[1], K. Bult[1]
[1]Broadcom, Bunnik, The Netherlands
[2]Wolfson Microelectronics, Edinburgh, United Kingdom

11.5 A 100MS/s 10.5b 2.46mW Comparator-less Pipeline ADC Using Self-Biased Ring Amplifiers — **10:45 AM**
Y. Lim[1,2], M. P. Flynn[1]
[1]University of Michigan, Ann Arbor, MI
[2]Samsung Electronics, Yongin, Korea

11.6 A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13μm CMOS with 74dB SNDR — **11:15 AM**
D-Y. Chang[1], C. Muñoz[2], D. Daly[2], S-K. Shin[2], K. Guay[2], T. Thurston[2], H-S. Lee[3], K. Gulati[1], M. Straayer[2]
[1]Maxim Integrated, San Jose, CA
[2]Maxim Integrated, North Chelmsford, MA
[3]Massachusetts Institute of Technology, Cambridge, MA

11.7 A 240mW 16b 3.2GS/s DAC in 65nm CMOS with <-80dBc IM3 up to 600MHz — **11:45 AM**
H. van de Vel, J. Briaire, C. Bastiaansen, P. van Beek, G. Geelen, H. Gunnink, Y. Jin, M. Kaba, K. Luo, E. Paulus, B. Pham, W. Relyveld, P. Zijlstra
Integrated Device Technology, Eindhoven, The Netherlands

Conclusion — **12:15 PM**

Sensors, MEMS and Displays

Session Chair: Ralf Brederlow, *Texas Instruments, Freising, Germany*
Associate Chair: Yoshiharu Nakajima, *Japan Display, Kanagawa, Japan*

12.1 3D Ultrasonic Gesture Recognition DS **8:30 AM**
R. J. Przybyla[1], H-Y. Tang[1], S. E. Shelton[2], D. A. Horsley[2], B. E. Boser[1]
[1]University of California, Berkeley, CA; [2]University of California, Davis, CA

12.2 3D Gesture-Sensing System for Interactive Displays Based on Extended-Range Capacitive Sensing DS **9:00 AM**
Y. Hu, L. Huang, W. Rieutort-Louis, J. Sanz-Robinson, S. Wagner, J. C. Sturm, N. Verma
Princeton University, Princeton, NJ

12.3 A 240Hz-Reporting-Rate 143×81 Mutual-Capacitance Touch-Sensing Analog Front-End IC with 37dB SNR for 1mm-Diameter Stylus DS **9:15 AM**
M. Hamaguchi[1], A. Nagao[2], M. Miyamoto[2]
[1]Sharp, Fukuyama, Japan; [2]Sharp, Tenri, Japan

12.4 A 1mm-Pitch 80×80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan DS **9:30 AM**
N. Miura[1], S. Dosho[2], S. Takaya[1], D. Fujimoto[1], T. Kiriyama[1], H. Tezuka[2], T. Miki[2], H. Yanagawa[2], M. Nagata[1]
[1]Kobe University, Kobe, Japan; [2]Panasonic, Osaka, Japan

Break **10:00 AM**

12.5 2D Coded-Aperture-Based Ultra-Compact Capacitive Touch-Screen Controller with 40 Reconfigurable Channels **10:15 AM**
H. Jang[1], H. Shin[2], S. Ko[1], I. Yun[2], K. Lee[1]
[1]KAIST, Daejeon, Korea; [2]Zinitix, Daejeon, Korea

12.6 A 160nW 63.9fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes **10:45 AM**
H. Ha[1], D. Sylvester[2], D. Blaauw[2], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]University of Michigan, Ann Arbor, MI

12.7 A 0.85V 600nW All-CMOS Temperature Sensor with an Inaccuracy of ±0.4°C (3σ) from -40 to 125°C **11:15 AM**
K. Souri[1], Y. Chae[2], F. Thus[3], K. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Yonsei University, Seoul, Korea
[3]NXP Semiconductors, Eindhoven, The Netherlands

12.8 A BJT-Based CMOS Temperature Sensor with a 3.6pJ·K²-Resolution FoM DS **11:30 AM**
A. Heidary[1,2,3], G. Wang[1,2], K. Makinwa[2], G. Meijer[1,2,4]
[1]Smartec, Breda, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
[3]Guilan University, Rasht, Iran; [4]SensArt, Delft, The Netherlands

12.9 A 1.55×0.85mm² 3ppm 1.0µA 32.768kHz MEMS-Based Oscillator **11:45 AM**
S. Zali Asl[1,2], S. Mukherjee[1], W. Chen[1], K. Joo[1], R. Palwai[1], N. Arumugam[1], P. Galle[1], M. Phadke[1], C. Grosjean[1], J. Salvia[1], H. Lee[1], S. Pamarti[3], T. Fiez[2], K. Makinwa[4], A. Partridge[1], V. Menon[1]
[1]SiTime, Sunnyvale, CA; [2]Oregon State University, Corvallis, OR
[3]University of California, Los Angeles, CA
[4]Delft University of Technology, Delft, The Netherlands

Conclusion **12:15 PM**

Advanced Embedded Memory

Session Chair: Jonathan Chang, *TSMC, Hsinchu, Taiwan*
Associate Chair: Hugh Mair, *MediaTek, Fairview, TX*

13.1 **A 1Gb 2GHz Embedded DRAM in 22nm Tri-Gate CMOS Technology** (DS) **1:30 PM**
F. Hamzaoglu, U. Arslan, N. Bisnik, S. Ghosh, M. B. Lal, N. Lindert, M. Meterelliyoz, R. B. Osborne, J. Park, S. Tomishima, Y. Wang, K. Zhang
Intel, Hillsboro, OR

13.2 **A 14nm FinFET 128Mb 6T SRAM with V_{MIN}-Enhancement Techniques for Low-Power Applications** **2:00 PM**
T. Song, W. Rim, J. Jung, G. Yang, J. Park, S. Park, K-H. Baek, S. Baek, S-K. Oh, J. Jung, S. Kim, G. Kim, J. Kim, Y. Lee, K. S. Kim, S-P. Sim, J. S. Yoon, K-M. Choi
Samsung Electronics, Yongin, Korea

13.3 **20nm High-Density Single-Port and Dual-Port SRAMs with Wordline-Voltage-Adjustment System for Read/Write Assists** **2:30 PM**
M. Yabuuchi, Y. Tsukamoto, M. Morimoto, M. Tanaka, K. Nii
Renesas Electronics, Tokyo, Japan

13.4 **A 7ns-Access-Time 25μW/MHz 128kb SRAM for Low-Power Fast Wake-Up MCU in 65nm CMOS with 27fA/b Retention Current** **2:45 PM**
T. Fukuda[1], K. Kohara[1], T. Dozaka[1], Y. Takeyama[1], T. Midorikawa[1], K. Hashimoto[2], I. Wakiyama[2], S. Miyano[1], T. Hojo[1]
[1]Toshiba, Kawasaki, Japan
[2]Toshiba Microelectronics, Kawasaki, Japan

Break **3:00 PM**

13.5 **A 16nm 128Mb SRAM in High-κ Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-V_{MIN} Applications** **3:15 PM**
Y-H. Chen, W-M. Chan, W-C. Wu, H-J. Liao, K-H. Pan, J-J. Liaw, T-H. Chung, Q. Li, G. H. Chang, C-Y. Lin, M-C. Chiang, S-Y. Wu, S. Natarajan, J. Chang
TSMC, Hsinchu, Taiwan

13.6 **A 28nm 400MHz 4-Parallel 1.6Gsearch/s 80Mb Ternary CAM** **3:45 PM**
K. Nii[1], T. Amano[2], N. Watanabe[2], M. Yamawaki[3], K. Yoshinaga[3], M. Wada[3], I. Hayashi[2]
[1]Renesas Electronics, Kodaira, Japan
[2]Renesas Electronics, Itami, Japan
[3]Renesas System Design, Itami, Japan

13.7 **A Reconfigurable Sense Amplifier with Auto-Zero Calibration and Pre-Amplification in 28nm CMOS** **4:15 PM**
B. Giridhar, N. Pinckney, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

13.8 **A 32kb SRAM for Error-Free and Error-Tolerant Applications with Dynamic Energy-Quality Management in 28nm CMOS** **4:45 PM**
F. Frustaci[1,2], M. Khayatzadeh[2], D. Blaauw[2], D. Sylvester[2], M. Alioto[3]
[1]University of Calabria, Cosenza, Italy
[2]University of Michigan, Ann Arbor, MI
[3]National University of Singapore, Singapore, Singapore

Conclusion **5:15 PM**

Millimeter-Wave/Terahertz Techniques

Session Chair: Ullrich Pfeiffer, *University of Wuppertal, Wuppertal, Germany*
Associate Chair: Brian Floyd, *North Carolina State University, Raleigh, NC*

14.1 A 0.9V 20.9dBm 22.3%-PAE E-Band Power Amplifier with Broadband Parallel-Series Power Combiner in 40nm CMOS — 1:30 PM
D. Zhao, P. Reynaert
KU Leuven, Leuven, Belgium

14.2 A 79GHz Phase-Modulated 4GHz-BW CW Radar TX in 28nm CMOS — 2:00 PM
V. Giannini[1], D. Guermandi[1], Q. Shi[1,2], K. Vaesen[1], B. Parvais[1], W. van Thillo[1], A. Bourdoux[1], C. Soens[1], J. Craninckx[1], P. Wambacq[1,2]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

14.3 A Push-Pull mm-Wave Power Amplifier with <0.8° AM-PM Distortion in 40nm CMOS — 2:30 PM
S. Kulkarni, P. Reynaert
KU Leuven, Leuven, Belgium

14.4 A Class F-1/F 24-to-31GHz Power Amplifier with 40.7% Peak PAE, 15dBm OP_{1dB}, and 50mW P_{sat} in 0.13μm SiGe BiCMOS — 2:45 PM
S. Y. Mortazavi, K-J. Koh
Virginia Polytechnic Institute, Blacksburg, VA

Break — 3:00 PM

14.5 A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13μm SiGe BiCMOS — DS 3:15 PM
U. R. Pfeiffer[1], Y. Zhao[1], J. Grzyb[1], N. Sarmah[1], R. Al Hadi[1], W. Förster[1], H. Rücker[2], B. Heinemann[2]
[1]University of Wuppertal, Wuppertal, Germany
[2]IHP, Frankfurt (Oder), Germany

14.6 A Scalable Terahertz 2D Phased Array with +17dBm of EIRP at 338GHz in 65nm Bulk CMOS — 3:45 PM
Y. Tousi, E. Afshari
Cornell University, Ithaca, NY

14.7 A 300GHz Frequency Synthesizer with 7.9% Locking Range in 90nm SiGe BiCMOS — 4:15 PM
P-Y. Chiang[1], Z. Wang[1], O. Momeni[2], P. Heydari[1]
[1]University of California, Irvine, CA
[2]University of California, Davis, CA

14.8 A 247-to-263.5GHz VCO with 2.6mW Peak Output Power and 1.14% DC-to-RF Efficiency in 65nm Bulk CMOS — 4:45 PM
M. Adnan, E. Afshari
Cornell University, Ithaca, NY

Conclusion — 5:15 PM

SESSION 15 — Tuesday February 11th, 1:30 PM

Digital PLLs

Session Chair: Anthony Hill, *Texas Instruments, Dallas, TX*
Associate Chair: Hiroo Hayashi, *Toshiba, Kawasaki, Japan*

15.1 **A 0.0066mm² 780μW Fully Synthesizable PLL with a Current-Output DAC and an Interpolative Phase-Coupled Oscillator Using Edge-Injection Technique** — **1:30 PM**
W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

15.2 **A 0.012mm² 3.1mW Bang-Bang Digital Fractional-N PLL with a Power-Supply-Noise Cancellation Technique and a Walking-One-Phase-Selection Fractional Frequency Divider** — **2:00 PM**
J. Liu, T-K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, H. Park
Samsung Electronics, Yongin, Korea

15.3 **A 2.4GHz ADPLL with Digital-Regulated Supply-Noise-Insensitive and Temperature-Self-Compensated Ring DCO** — **2:15 PM**
Y-C. Huang, C-F. Liang, H-S. Huang, P-Y. Wang, MediaTek, Hsinchu, Taiwan

15.4 **A 20-to-1000MHz ±14ps Peak-to-Peak Jitter Reconfigurable Multi-Output All-Digital Clock Generator Using Open-Loop Fractional Dividers in 65nm CMOS** — **2:30 PM**
A. Elkholy[1], A. Elshazly[2], S. Saxena[1], G. Shu[1], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL; [2]Intel, Hillsboro, OR

Break — **3:00 PM**

SESSION 16 — Tuesday February 11th, 3:15 PM

SoC Building Blocks

Session Chair: Kathy Wilcox, *AMD, Boxborough, MA*
Associate Chair: Yasuhisa Shimazaki, *Renesas, Tokyo, Japan*

16.1 **A 340mV-to-0.9V 20.2Tb/s Source-Synchronous Hybrid Packet/Circuit-Switched 16×16 Network-on-Chip in 22nm Tri-Gate CMOS** — DS **3:15 PM**
G. Chen, M. A. Anders, H. Kaul, S. K. Satpathy, S. K. Mathew, S. K. Hsu, A. Agarwal, R. K. Krishnamurthy, S. Borkar, V. De
Intel, Hillsboro, OR

16.2 **A 0.19pJ/b PVT-Variation-Tolerant Hybrid Physically Unclonable Function Circuit for 100% Stable Secure Key Generation in 22nm CMOS** — **3:45 PM**
S. K. Mathew, S. K. Satpathy, M. A. Anders, H. Kaul, S. K. Hsu, A. Agarwal, G. K. Chen, R. J. Parker, R. K. Krishnamurthy, V. De
Intel, Hillsboro, OR

16.3 **A 23Mb/s 23pJ/b Fully Synthesized True-Random-Number Generator in 28nm and 65nm CMOS** — **4:15 PM**
K. Yang, D. Fick, M. B. Henry, Y. Lee, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

16.4 **0.6-to-1.0V 279μm², 0.92μW Temperature Sensor with Less Than +3.2/-3.4°C Error for On-Chip Dense Thermal Monitoring** — **4:45 PM**
T. Yang, S. Kim, P. R. Kinget, M. Seok, Columbia University, New York, NY

Conclusion — **5:15 PM**

Analog Techniques

Session Chair: Marco Berkhout, *NXP Semiconductors, Nijmegen, The Netherlands*
Associate Chair: Edgar Sanchez-Sinencio, *Texas A&M University, College Station, TX*

17.1 **An Integrated 80V 45W Class-D Power Amplifier with Optimal-Efficiency-Tracking Switching Frequency Regulation** **1:30 PM**
H. Ma, R. van der Zee, B. Nauta, University of Twente, Enschede, The Netherlands

17.2 **A 0.0013mm² 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin** **2:00 PM**
Z. Yan[1], P-I. Mak[1,2], M-K. Law[1,2], R. Martins[1,2,3], F. Maloberti[4]
[1]University of Macau, Macao, China; [2]UMTEC, Macao, China
[3]Instituto Superior Tecnico, Lisbon, Portugal; [4]University of Pavia, Pavia, Italy

17.3 **A 0.9V 6.3μW Multistage Amplifier Driving 500pF Capacitive Load with 1.34MHz GBW** **2:15 PM**
W. Qu, J-P. Im, H-S. Kim, G-H. Cho, KAIST, Daejeon, Korea

17.4 **CMOS Impedance Analyzer for Nanosamples Investigation Operating up to 150MHz with Sub-aF Resolution** DS **2:30 PM**
G. Ferrari, D. Bianchi, A. Rottigni, M. Sampietro
Politecnico di Milano, Milan, Italy

Break **3:00 PM**

17.5 **A 0.07mm² 2-Channel Instrumentation Amplifier with 0.1% Gain Matching in 0.16μm CMOS** **3:15 PM**
F. Sebastiano[1,2], F. Butti[3], R. van Veldhoven[1], P. Bruschi[3]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
[3]University of Pisa, Pisa, Italy

17.6 **Envelope Modulator for Multimode Transmitters with AC-Coupled Multilevel Regulators** **3:30 PM**
P. Arnò[1], M. Thomas[2,3], V. Molata[2,3], T. Jeřábek[2]
[1]STMicroelectronics, Grenoble, France
[2]STMicroelectronics, Prague, Czech Republic
[3]Czech Technical University, Prague, Czech Republic

17.7 **A 1.89nW/0.15V Self-Charged XO for Real-Time Clock Generation** **3:45 PM**
K-J. Hsiao, MediaTek
Hsinchu, Taiwan

17.8 **A 190nW 33kHz RC Oscillator with ±0.21% Temperature Stability and 4ppm Long-Term Stability** **4:00 PM**
D. Griffith[1], P. T. Røine[2], J. Murdock[1], R. Smith[1]
[1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Oslo, Norway

17.9 **A 0.6V 70MHz 4th-Order Continuous-Time Butterworth Filter with 55.8dB SNR, 60dB THD at +2.8dBm Output Signal Power** **4:15 PM**
J. N. Kuppambatti, B. Vigraham, P. R. Kinget
Columbia University, New York, NY

17.10 **0.65V-Input-Voltage 0.6V-Output-Voltage 30ppm/°C Low-Dropout Regulator with Embedded Voltage Reference for Low-Power Biomedical Systems** **4:45 PM**
W-C. Chen, Y-P. Su, Y-H. Lee, C-L. Wey, K-H. Chen
National Chiao Tung University, Hsinchu, Taiwan

17.11 **A 0.65ns-Response-Time 3.01ps FOM Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power-Supply-Rejection for Wideband Communication Systems** **5:00 PM**
Y. Lu, W-H. Ki, C. P. Yue
Hong Kong University of Science and Technology, Hong Kong, China

Conclusion **5:15 PM**

TIMETABLE OF ISSCC 2014 SESSIONS

Sunday, February 9th	ISSCC 2014 TUTORIALS		
8:30AM	**T1:** Filtering in RF Transceivers	**T2:** V(min) Constraints and Optimization in VLSI Circuit Design	**T3:** 3D Integration, Power Delivery, and Contactless Interconnect by Near Field Coupling
10:30AM	**T4:** Power Optimized Processor Design	**T5:** Peripheral Circuits for Analog-to-Digital Converters	**T6**: Analog Front-End Design for Gb/s Wireline Receivers
1:30PM	**T7:** Self-Adapting Design Techniques for Power Constrained Processors	**T8:** Interference Robust CMOS Radio Receiver Techniques	
3:30PM	**T9**: Charge Pump and Capacitive DCDC Converter Design	**T10:** Design of Physical-to-Digital Converters	
	ISSCC 2014 FORUMS		
8:00AM	**F1:** Digitally-Assisted Analog and Analog-Assisted Digital in High-Performance Scaled CMOS Process	**F2:** 3D Stacking Technologies for Image Sensors & Memories	

Events below in Bold Box included in Conference registration

	ISSCC 2014 EVENING SESSIONS	
	7:30 PM ES1: Student Research Preview: Short Presentations with Poster Session	**8:00 PM ES2:** Data Centers to Support Tomorrow's Cloud

Monday, February 10th	ISSCC 2014 PAPER SESSIONS				
8:30AM	**Session 1:** Plenary Session				
1:30PM	**Session 2:** Ultra High-Speed Wireline Transceiver & Techniques	**Session 3:** RF Techniques	**Session 4:** DC-DC Converters	**Session 5:** Processors	**Session 6:** Technologies for High-Speed Data Networks **Session 7:** Image Sensors
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour				
	ISSCC 2014 SESSIONS				
8:00PM	**EP1: Plenary Roundtable : Next-Generation Networked Systems - Challenges for Silicon**				

Tuesday, February 11th	ISSCC 2014 PAPER SESSIONS				
8:30AM	**Session 8:** Optical Links and Copper PHYs	**Session 9:** Low-Power Wireless	**Session 10:** Mobile System-on-Chip (SoCs)	**Session 11:** Data Converter Techniques	**Session 12:** Sensors, MEMs, and Displays
1:30PM	**Session 13:** Advanced Embedded Memory	**Session 14:** Millimeter-Wave / Terahertz Techniques	**Session 15:** Digital PLLs **Session 16:** SoC Building Blocks	**Session 17:** Analog Techniques	**Session 18:** Biomedical Systems for Improved Quality of Life
5:15PM	Author Interviews, Social Hour				
	ISSCC 2014 EVENING SESSIONS				
8:00PM	**ES3:** Wearable Wellness Devices: Fashion, Health, & Informatics	**EP2:** Anatomy of Innovation: Bug or Feature?		**EP3:** Perspectives on the Future of Semiconductor Innovation	

Wednesday, February 12th	ISSCC 2014 PAPER SESSIONS				
8:30AM	**Session 19:** Nonvolatile Memory	**Session 20:** Wireless Systems	**Session 21:** Frequency Generation Techniques	**Session 22:** High-Speed Data Converters	**Session 23:** Energy Harvesting
1:30PM	**Session 24:** Integrated Biomedical Systems	**Session 25:** High-Bandwidth Low-Power DRAM and I/O **Session 26:** Energy-Efficient Dense Interconnect	**Session 27:** Energy-Efficient Digital Circuits	**Session 28:** Mixed-Signal Techniques for Wireless **Session 29:** Data Converters for Wireless Systems	**Session 30:** Technologies for Next-Generation Systems
5:15 PM	Author Interviews				

Thursday, February 13th	ISSCC 2014 SHORT COURSE			
8:00 AM	**SC1:** Biomedical and Sensor Interface Circuits			
	ISSCC 2014 FORUMS			
8:00AM	**F3:** Adaptive Design Techniques for Energy Efficiency	**F4:** mm-Wave Advances for Active Safety and Communication Systems	**F5:** Low Power Radios for Sensor Networks	**F6:** Energy Efficient I/O Design for Next-Generation Systems

Biomedical Systems for Improved Quality of Life

Session Chair: Yogesh Ramadass, *Texas Instruments, Dallas, TX*
Associate Chair: David Ruffieux, *CSEM, Neuchatel, Switzerland*

18.1 A 1V 3mA 2.4GHz Wireless Digital Audio Communication SoC for Hearing-Aid Applications in 0.18µm CMOS DS 1:30 PM

A. El-Hoiydi[1], F. Callias[1], Y. Oesch[1], C. Kuratli[2], R. Kvacek[3]
[1]Phonak Communications, Murten, Switzerland
[2]EM Microelectronic, Marin, Switzerland
[3]ASICentrum, Prague, Czech Republic

18.2 A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18µm HVCMOS DS 2:00 PM

M. Yip[1], R. Jin[1], H. H. Nakajima[2,3], K. M. Stankovic[2,3], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Harvard Medical School, Boston, MA
[3]Massachusetts Eye and Ear Infirmary, Boston, MA

18.3 A Multi-Parameter Signal-Acquisition SoC for Connected Personal Health Applications DS 2:30 PM

N. van Helleputte[1], M. Konijnenburg[2], H. Kim[1], J. Pettine[2], D-W. Jee[1], A. Breeschoten[2], A. Morgado[1], T. Torfs[1], H. de Groot[2], C. van Hoof[1], R. F. Yazicioglu[1]
[1]imec, Leuven, Belgium
[2]Holst Centre/imec, Eindhoven, The Netherlands

Break 3:00 PM

18.4 A 4.9mΩ-Sensitivity Mobile Electrical Impedance Tomography IC for Early Breast-Cancer Detection System 3:15 PM

S. Hong, K. Lee, U. Ha, H. Kim, Y. Lee, Y. Kim, H-J. Yoo
KAIST, Daejeon, Korea

18.5 A 2.14mW EEG Neuro-Feedback Processor with Transcranial Electrical Stimulation for Mental-Health Management 3:45 PM

T. Roh, K. Song, H. Cho, D. Shin, U. Ha, K. Lee, H-J. Yoo
KAIST, Daejeon, Korea

18.6 2.5D Heterogeneously Integrated Bio-Sensing Microsystem for Multi-Channel Neural-Sensing Applications 4:15 PM

P-T. Huang[1], L-C. Chou[1], T-C. Huang[1], S-L. Wu[1], T-S. Wang[1], Y-R. Lin[1], C-A. Cheng[1], W-W. Shen[1], K-N. Chen[1], J-C. Chiou[1,2], C-T. Chuang[1], W. Hwang[1], K-H. Chen[3], C-T. Chiu[3], M-H. Cheng[3], Y-L. Lin[3], H-M. Tong[3]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]China Medical University, Taichung, Taiwan
[3]Advanced Semiconductor Engineering Group, Kaohsiung, Taiwan

18.7 A Remotely Controlled Locomotive IC Driven by Electrolytic Bubbles and Wireless Powering 4:45 PM

P-H. Kuo[1], J-Y. Hsieh[1], Y-C. Huang[1], Y-J. Huang[1], R-D. Tsai[2], T. Wang[3], H-W. Chiu[2], S-S. Lu[1]
[1]National Taiwan University, Taipei, Taiwan
[2]National Taipei University of Technology, Taipei, Taiwan
[3]Chang Gung University, Taoyuan, Taiwan

Conclusion 5:15 PM

ES3: Wearable Wellness Devices: Fashion, Health, and Informatics

Organizers: **Firat Yazicioglu,** *imec, Leuven, Belgium*
Sam Kavusi, *Bosch Research, Palo Alto, CA*

Chair: **Chris Van Hoof,** *imec, Leuven, Belgium*

Imagine using the same device for fashion/style and for monitoring your wellness? What about a tattoo of your child's name that also tracks your fitness and activity level. Can we make contact lenses that can change the color of your eyes but also see the calorie content of your lunch box?

Early prototypes of such devices are already emerging. Smart contact lenses can display words or images in your line of sight, and stretchable/tattoo electronics can monitor vital signs. However, there are significant design and technology challenges ahead to actually make these devices fully functional, autonomous, and reliable.

Let's hear from the experts what could be the future of wearable wellness devices and what technologies are being developed.

Time	Topic
8:00	**Stretchable Electronics: Biointegrated Systems with Unusual Materials and Designs** ***Roozbeh Ghaffari,*** *MC10, Cambridge, MA*
8:25	**Smart Textiles for Wearable Electronics** ***Jerald Yoo,*** *Masdar Inst. of Sci. and Tech, Abu Dhabi, UAE*
8:50	**Extremely Low-Power Circuit Design for Wearable Systems** **Makoto Takamiya,** *University of Tokyo, Tokyo, Japan*
9:15	**Smart Contact Lenses and Integrated Circuits** **Jelle De Smet,** *Ghent University, Ghent, Belgium*
9:40	**Energy Harvesting for Wearable Systems** **Yiannos Manoli,** *University of Freiburg and HSG-IMIT, Freiburg, Germany*
10:05	**Conclusion**

EP2: Anatomy of Innovation: Bug or Feature?

Organizer: **Harry Lee,** *MIT, Cambridge, MA*
Co-Organizer: **Ken Nishimura,** *Agilent Technologies, Santa Clara, CA*

Moderator: **Harry Lee,** *MIT, Cambridge, MA*

As process scaling slows down, circuit innovation is becoming one of the most important differentiators. We can point to great inventions of the past that were accidental, or failed attempts to solve other problems (bugs), as well as those from logical thinking (features). Which is more effective? In this panel, top analog circuit innovators describe the process by which their best innovations were conceived. They give interesting examples, such as turning a bug in the circuit into a feature. Then they argue whether innovation is more effective as a result of accidental discovery or logical thinking.

Panelists:
Ali Hajimiri, *CalTech, Pasadena, CA*
Qiuting Huang, *Swiss Federal Inst of Tech (ETH), Zürich, Switzerland*
Lawrence Loh, *MediaTek, Hsinchu, Taiwan*
Kofi Makinwa, *Delft University of Technology, Delft, Netherlands*,
Akira Matsuzawa, *Tokyo Institute of Technology, Tokyo, Japan*,
Dennis Monticelli, *Texas Instruments, Santa Clara, CA*

EP3: Perspectives on the Future of Semiconductor Innovation

Organizers: **Chris Nicol,** *Wave Semiconductor, Sunnyvale, CA*
Ali Keshavarzi, *Cypress Semiconductor, San Jose, CA*

Moderators: **Ali Keshavarzi,** *Cypress Semiconductor, San Jose, CA*
Chris Nicol, *Wave Semiconductor, Sunnyvale, CA*

In a "call for leadership" panel at ISSCC, we will be seeking leaders' perspectives on the future of discontinuous innovation in the semiconductor industry. An ensemble of visionaries, experts and CEOs will discuss the opportunities and challenges for innovation in our industry. Of primary concern is the reduction in funding available for new semiconductor ventures. Are the escalating NRE costs of ASICs providing a barrier to new entrants? What advice would our distinguished panellists give to entrepreneurs thinking of starting a new semiconductor company?

We believe that significant innovation is needed across a broad spectrum of technologies to fuel the insatiable demand for enhanced user experiences in portable systems. For mobile computing, any slowdown in MIPS/W improvement will require a faster rate of improvement in the energy density (Wh/L) of battery technology. For cloud services, the cost of power delivery and cooling is a significant % of operating expenditures and needs to be reduced to sustain growth. In these applications, lack of semiconductor innovation will result in anaemic improvement in MIPS/W/$ and will therefore impact the growth rate of mobile and cloud computing. This panel contains representatives from service and system providers and we will ask them if their future needs are likely to be met by current silicon roadmaps or if increased investment in semiconductor innovation is required.

Many of the semiconductor platforms for future systems will be delivered by Multi-National Corporations (MNCs). The panel contains CEOs from semiconductor MNCs and we will ask them if they are increasing their investment in innovation or if a strategy of acquisition is a sustainable innovation strategy going forward. It is possible that the VCs will have something to say on this matter.

Are funding sources (and incentives) in offshore markets shifting the focus of semiconductor innovation to nations like China, Brazil and Russia or regions like The Middle East? Are there pitfalls with this trend? Should Government do more to support small companies? If public-funded institutes and universities provide the research, must they fund the commercialization of this research into semiconductor products? Is the fabless semi model being displaced by the IP model? And many more unlisted questions that will be discussed in front of an ISSCC audience consisting of experts in the field, inventors, startups, researchers, young professionals and the students that will fuel the future of the industry. We believe that this issue being debated in our panel is serious, and affects everybody working in, or considering a career in the semiconductor industry. We therefore have extended our call for leadership to discuss these issues that will shape the future of the innovation landscape in our industry.

Panelists:

Nicky Lu, *Etron, Hsinchu, Taiwan*
Scott McGregor, *Broadcom, Irvine, CA*
T.J. Rodgers, *Cypress Semiconductor, San Jose, CA*
Simon Segars, *ARM, Cambridge, United Kingdom*
Luc Van den hove, *imec, Heverlee, Belgium*
Dado Banatao, *Tallwood, Menlo Park, CA*
John Doerr, *KPCB, Menlo Park, CA*
Andy Rappaport, *August Capital, Menlo Park, CA*

Nonvolatile Memory Solutions

Session Chair: Jin-Man Han, *Samsung Electronics, Hwaseong, Korea*
Associate Chair: Tadaaki Yamauchi, *Renesas Electronics, Tokyo, Japan*

19.1 A 128Gb MLC NAND-Flash Device Using 16nm Planar Cell **8:30 AM**
M. Helm[1], J-K. Park[1], A. Ghalam[1], J. Guo[1], C. W. Ha[1], C. Hu[1], H. Kim[1], K. Kavalipurapu[1], E. Lee[1], A. Mohammadzadeh[1], D. Nguyen[1], V. Patel[1], T. Pekny[1], B. Saiki[1], D. Song[1], J. Tsai[1], V. Viajedor[1], L. Vu[1], T. Wong[1], J. H. Yun[1], R. Ghodsi[1], A. D'Alessandro[2], D. Di Cicco[2], V. Moschiano[2]
[1]Micron, San Jose, CA; [2]Micron, Avezzano, Italy

19.2 A 93.4mm² 64Gb MLC NAND-Flash Memory with 16nm CMOS Technology **9:00 AM**
S. Choi, D. Kim, S. Choi, B. Kim, S. Jung, K. Chun, N. Kim, W. Lee, T. Shin, H. Jin, H. Cho, S. Ahn, Y. Hong, I. Yang, B. Kim, P. Yoo, Y. Jung, J. Lee, J. Shin, T. Kim, K. Park, J. Kim
SK Hynix, Icheon, Korea

19.3 66.3KIOPS-Random-Read 690MB/s-Sequential-Read Universal Flash Storage Device Controller with Unified Memory Extension **9:30 AM**
K. Watanabe[1], K. Yoshii[1], N. Kondo[1], K. Maeda[1], T. Fujisawa[1], J. Wadatsumi[2], D. Miyashita[2], S. Kousai[2], Y. Unekawa[2], S. Fujii[2], T. Aoyama[2], T. Tamura[1], A. Kunimatsu[1], Y. Oowaki[1]
[1]Toshiba, Yokohama, Japan; [2]Toshiba, Kawasaki, Japan

Break **10:00 AM**

19.4 Embedded 1Mb ReRAM in 28nm CMOS with 0.27-to-1V Read Using Swing-Sample-and-Couple Sense Amplifier and Self-Boost-Write-Termination Scheme **10:15 AM**
M-F. Chang[1], J-J. Wu[1], T-F. Chien[1], Y-C. Liu[1], T-C. Yang[1], W-C. Shen[1], Y -C. King[1], C-J. Lin[1], K-F. Lin[2], Y-D. Chih[2], S. Natarajan[2], J. Chang[2]
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

19.5 Three-Dimensional 128Gb MLC Vertical NAND Flash-Memory with 24-WL Stacked Layers and 50MB/s High-Speed Programming **10:45 AM**
K-T. Park, J-M. Han, D. Kim, S. Nam, K. Choi, M-S. Kim, P. Kwak, D. Lee, Y-H. Choi, K-M. Kang, M-H. Choi, D-H. Kwak, H-W. Park, S-W. Shim, H-J. Yoon, D. Kim, S-W. Park, K. Lee, K. Ko, D-K. Shim, Y-L. Ahn, J. Park, J. Ryu, D. Kim, K. Yun, J. Kwon, S. Shin, D. Youn, W-T. Kim, T. Kim, S-J. Kim, S. Seo, H-G. Kim, D-S. Byeon, H-J. Yang, M. Kim, M-S. Kim, J. Yeon, J. Jang, H-S. Kim, W. Lee, D. Song, S. Lee, K-H. Kyung, J-H. Choi
Samsung Semiconductor, Hwasung, Korea

19.6 Hybrid Storage of ReRAM/TLC NAND Flash with RAID-5/6 for Cloud Data Centers **11:15 AM**
S. Tanakamaru[1,2], H. Yamazawa[1], T. Tokutomi[1], S. Ning[1,2], K. Takeuchi[1]
[1]Chuo University, Tokyo, Japan
[2]University of Tokyo, Tokyo, Japan

19.7 A 16Gb ReRAM with 200MB/s Write and 1GB/s Read in 27nm Technology **11:45 AM**
R. Fackenthal[1], M. Kitagawa[2], W. Otsuka[2], K. Prall[3], D. Mills[1], K. Tsutsui[4], J. Javanifard[1], K. Tedrow[1], T. Tsushima[2], Y. Shibahara[4], G. Hush[3]
[1]Micron, Folsom, CA; [2]Sony, Boise, ID; [3]Micron, Boise, ID; [4]Sony, Kanagawa, Japan

Conclusion **12:15 PM**

Wireless Systems

Session Chair: Iason Vassiliou, *Broadcom, Alimos, Greece*
Associate Chair: Myung-Woon Hwang, *FCI, Sungnam, Korea*

20.1 A 40nm CMOS Receiver for 60GHz Discrete-Carrier Indoor Localization Achieving mm-Precision at 4m Range — **8:30 AM**
T. Redant, T. Ayhan, N. De Clercq, M. Verhelst, P. Reynaert, W. Dehaene
KU Leuven, Leuven, Belgium

20.2 A 16TX/16RX 60GHz 802.11ad Chipset with Single Coaxial Interface and Polarization Diversity — **9:00 AM**
M. Boers[1], I. Vassiliou[2], S. Sarkar[1], S. Nicolson[1], E. Adabi[1], B. Afshar[1], B. Perumana[1], T. Chalvatzis[2], S. Kavadias[2], P. Sen[1], W. L. Chan[1], A. Yu[1], A. Parsa[3], M. Nariman[1], S. Yoon[1], A. Grau Besoli[1], C. Kyriazidou[2], G. Zochios[2], N. Kocaman[1], A. Garg[1], H. Eberhart[1], P. Yang[1], H. Xie[1], H. J. Kim[1], A. Tarighat[1], D. Garrett[1], A. Blanksby[1], M. K. Wong[4], D. P. Thirupathi[1], S. Mak[3], R. Srinivasan[1], A. Ibrahim[1], E. Sengul[1], V. Roussel[1], P-C. Huang[1], T. Yeh[3], M. Mese[1], J. Castaneda[1], B. Ibrahim[1], T. Sowlati[1], M. Rofougaran[1], A. Rofougaran[1]
[1]Broadcom, Irvine, CA; [2]Broadcom, Alimos, Greece
[3]Broadcom, San Diego, CA; [4]Broadcom, Sunnyvale, CA

20.3 A 64-QAM 60GHz CMOS Transceiver with 4-Channel Bonding — **9:30 AM**
K. Okada, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, S. Kondo, T. Ueno, Y. Takeuchi, T. Yamaguchi, A. Musa, R. Wu, M. Miyahara, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

Break — **10:00 AM**

20.4 A Fully Integrated Single-Chip 60GHz CMOS Transceiver with Scalable Power Consumption for Proximity Wireless Communication — **10:15 AM**
S. Saigusa, T. Mitomo, H. Okuni, M. Hosoya, A. Sai, S. Kawai, T. Wang, M. Furuta, K. Shiraishi, K. Ban, S. Horikawa, T. Tandai, R. Matsuo, T. Tomizawa, H. Hoshino, J. Matsuno, Y. Tsutsumi, R. Tachibana, O. Watanabe, T. Itakura
Toshiba, Kawasaki, Japan

20.5 A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput — DS — **10:30 AM**
M. He, R. Winoto, X. Gao, W. Loeb, D. Signoff, W. Lau, Y. Lu, D. Cui, K-S. Lee, S-W. Tam, P. Godoy, Y. Chen, S. Joo, C. Hu, A. A. Paramanandam, X. Wang, C-H. Lin, L. Lin
Marvell, Santa Clara, CA

20.6 A Blocker-Resilient Wideband Receiver with Low-Noise Active Two-Point Cancellation of >0dBm TX Leakage and TX Noise in RX Band for FDD/Co-Existence — **10:45 AM**
J. Zhou, P. R. Kinget, H. Krishnaswamy,
Columbia University, New York, NY

20.7 A Multi-Band Inductor-Less SAW-Less 2G/3G-TD-SCDMA Cellular Receiver in 40nm CMOS — **11:15 AM**
M-D. Tsai, C-F. Liao, C-Y. Wang, Y-B. Lee, B. Tzeng, G-K. Dehng
MediaTek, Hsinchu, Taiwan

20.8 A 20mW GSM/WCDMA Receiver with RF Channel Selection — **11:45 AM**
J. W. Park, B. Razavi, University of California, Los Angeles, CA

Conclusion — **12:15 PM**

Frequency Generation Techniques

Session Chair: Piet Wambacq, *imec, Heverlee, Belgium*
Associate Chair: Chih-Ming Hung, *MStar Semiconductor, Taipei, Taiwan*

21.1 A 1.7GHz MDLL-Based Fractional-N Frequency Synthesizer with 1.4ps RMS Integrated Jitter and 3mW Power Using a 1b TDC — **8:30 AM**
G. Marucci, A. Fenaroli, G. Marzin, S. Levantino, C. Samori, A. L. Lacaita
Politecnico di Milano, Milan, Italy

21.2 A 2.3GHz Fractional-N Dividerless Phase-Locked Loop with -112dBc/Hz In-Band Phase Noise — **9:00 AM**
P-C. Huang, W-S. Chang, T-C. Lee
National Taiwan University, Taipei, Taiwan

21.3 A 2GHz 130mW Direct-Digital Frequency Synthesizer with a Nonlinear DAC in 55nm CMOS — **9:30 AM**
T. Yoo[1], Y-H. Jung[1], H. C. Yeoh[1,2], Y. S. Kim[1], S-M. Kang[3], K-H. Baek[1]
[1]Chung-Ang University, Seoul, Korea
[2]Analog Devices, San Jose, CA
[3]KAIST, Daejeon, Korea

Break — **10:00 AM**

21.4 A 42mW 230fs-Jitter Subsampling 60GHz PLL in 40nm CMOS — **10:15 AM**
V. Szortyka[1,2], Q. Shi[1,2], K. Raczkowski[1], B. Parvais[1], M. Kuijk[2], P. Wambacq[1,2]
[1]imec, Heverlee, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

21.5 A 3.24-to-8.45GHz Low-Phase-Noise Mode-Switching Oscillator — **10:45 AM**
M. Taghivand[1,2], K. Aggarwal[1], A. S. Y. Poon[1]
[1]Stanford University, Stanford, CA
[2]Qualcomm, San Jose, CA

21.6 A 2.4-to-5.3GHz Dual-Core CMOS VCO with Concentric 8-Shaped Coils — **11:00 AM**
L. Fanori[1,], T. Mattsson[2], P. Andreani[1,2]*
[1]Lund University, Lund, Sweden
[*]now with Marvell, Pavia, Italy
[2]Ericsson, Lund, Sweden

21.7 A 1.8mW PLL-Free Channelized 2.4GHz ZigBee Receiver Utilizing Fixed-LO Temperature-Compensated FBAR Resonator — **11:15 AM**
K. Wang[1], J. Koo[1], R. Ruby[2], B. Otis[1]
[1]University of Washington, Seattle, WA
[2]Avago Technologies, San Jose, CA

21.8 A Pulling Mitigation Technique for Direct-Conversion Transmitters — **11:45 AM**
A. Mirzaei, M. Mikhemar, H. Darabi
Broadcom, Irvine, CA

Conclusion — **12:15 PM**

High-Speed Data Converters

Session Chair: Jieh-Tsorng Wu, *National Chiao Tung University, Hsinchu, Taiwan*
Associate Chair: Seung-Tak Ryu, *KAIST, Daejeon, Korea*

22.1 A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS — **8:30 AM**
L. Kull[1,2], T. Toifl[1], M. Schmatz[1], P. A. Francese[1], C. Menolfi[1], M. Braendli[1], M. Kossel[1], T. Morf[1], T. M. Andersen[1], Y. Leblebici[2]
[1]IBM Research, Rüschlikon, Switzerland
[2]EPFL, Lausanne, Switzerland

22.2 A 69.5mW 20GS/s 6b Time-Interleaved ADC with Embedded Time-to-Digital Calibration in 32nm CMOS SOI — **9:00 AM**
V. H-C. Chen, L. Pileggi
Carnegie Mellon University, Pittsburgh, PA

22.3 A 20GHz-BW 6b 10GS/s 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology — **9:30 AM**
S. Le Tual[1], P. N. Singh[2], C. Curis[3], P. Dautriche[1]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Greater Noida, India
[3]STMicroelectronics, Grenoble, France

Break — **10:00 AM**

22.4 A 1GS/s 10b 18.9mW Time-Interleaved SAR ADC with Background Timing-Skew Calibration — **10:15 AM**
S. Lee, A. P. Chandrakasan, H-S. Lee
Massachusetts Institute of Technology, Cambridge, MA

22.5 A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS — DS — **10:45 AM**
N. Le Dortz[1,2], J-P. Blanc[1], T. Simon[1], S. Verhaeren[1], E. Rouat[1], P. Urard[1], S. Le Tual[1], D. Goguet[1], C. Lelandais-Perrault[2], P. Benabes[2]
[1]STMicroelectronics, Crolles, France
[2]Supélec, Gif-sur-Yvette, France

22.6 A 2.2GS/s 7b 27.4mW Time-Based Folding-Flash ADC with Resistively Averaged Voltage-to-Time Amplifiers — **11:15 AM**
M. Miyahara, I. Mano, M. Nakayama, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

22.7 A 14b 4.6GS/s RF DAC in 0.18µm CMOS for Cable Head-End Systems — **11:45 AM**
B. Brandt[1], D. McMahill[2], M. Wu[1], P. Kalthoff[3], A. Kuckreja[4], G. Ostrem[3]
[1]Maxim Integrated, North Chelmsford, MA
[2]Maxim Integrated, Woodstock, GA
[3]Maxim Integrated, Colorado Springs, CO
[4]Maxim Integrated, Boulder, CO

Conclusion — **12:15 PM**

Energy Harvesting

Session Chair: Makoto Nagata, *Kobe University, Kobe, Japan*
Associate Chair: Tsung-Hsien Lin, *National Taiwan University, Taipei, Taiwan*

23.1 A 0.15V-Input Energy-Harvesting Charge Pump with Switching Body Biasing and Adaptive Dead-Time for Efficiency Improvement — **8:30 AM**
J. Kim[1,2], P. K. T. Mok[1], C. Kim[2]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Korea University, Seoul, Korea

23.2 A 1.1nW Energy Harvesting System with 544pW Quiescent Power for Next-Generation Implants — **9:00 AM**
S. Bandyopadhyay[1,], P. P. Mercier[1,2], A. C. Lysaght[3], K. M. Stankovic[3,4], A. P. Chandrakasan[1]*
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]University of California, San Diego, La Jolla, CA
[3]Massachusetts Eye and Ear Infirmary, Boston, MA
[4]Massachusetts General Hospital, Harvard Medical School, Boston, MA
[*]now at Texas Instruments, Dallas, TX

23.3 A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter — **9:30 AM**
W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

Break — **10:00 AM**

23.4 Dual-Source Single-Inductor 0.18µm CMOS Charger-Supply with Nested Hysteretic and Adaptive On-Time PWM Control — **10:15 AM**
S. Kim, G. A. Rincón-Mora
Georgia Institute of Technology, Atlanta, GA

23.5 An Energy Pile-Up Resonance Circuit Extracting Maximum 422% Energy from Piezoelectric Material in a Dual-Source Energy-Harvesting Interface — **10:45 AM**
Y-S. Yuk, S. Jung, H-D. Gwon, S. Choi, S. D. Sung, T-H. Kong, S-W. Hong, J-H. Choi, M-Y. Jeong, J-P. Im, S-T. Ryu, G-H. Cho
KAIST, Daejeon, Korea

23.6 A 43V 400mW-to-21W Global-Search-Based Photovoltaic Energy Harvester with 350µs Transient Time, 99.9% MPPT Efficiency, and 94% Power Efficiency — **11:15 AM**
S. Uprety, H. Lee
University of Texas, Dallas, Richardson, TX

23.7 Self-Powered 30µW-to-10mW Piezoelectric Energy-Harvesting System with 9.09ms/V Maximum Power Point Tracking Time — **11:45 AM**
M. Shim, J. Kim, J. Jung, C. Kim
Korea University, Seoul, Korea

23.8 A 34V Charge Pump in 65nm Bulk CMOS Technology — **12:00 PM**
Y. Ismail[1], H. Lee[2,], S. Pamarti[1], C-K. K. Yang[1]*
[1]University of California, Los Angeles, CA
[2]SiTime, Sunnyvale, CA
[*]now with Altera, San Jose, CA

Conclusion — **12:15 PM**

Integrated Biomedical Systems

Session Chair: Maysam Ghovanloo, *Georgia Institute of Technology, Atlanta, GA*
Associate Chair: Wentai Liu, *University of California, Los Angeles, CA*

24.1 A Miniaturized 64-Channel 225μW Wireless Electrocorticographic Neural Sensor **1:30 PM**
R. Muller[1,2], H-P. Le[1], W. Li[1], P. Ledochowitsch[1], S. Gambini[2], T. Bjorninen[3], A. Koralek[1], J. M. Carmena[1], M. M. Maharbiz[1], E. Alon[1], J. M. Rabaey[1]
[1]University of California, Berkeley, CA; [2]University of Melbourne, Parkville, Australia
[3]Tampere University of Technology, Tampere, Finland

24.2 A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep-Brain Stimulation **2:00 PM**
H-M. Lee[1], K-Y. Kwon[2], W. Li[2], M. Ghovanloo[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Michigan State University, East Lansing, MI

24.3 An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis **2:30 PM**
D. Jeon[1], Y-P. Chen[1], Y. Lee[1], Y. Kim[1], Z. Foo[1], G. Kruger[1], H. Oral[2], O. Berenfeld[2], Z. Zhang[1], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI
[2]University of Michigan Health System, Ann Arbor, MI

Break **3:00 PM**

24.4 A 680nA Fully Integrated Implantable ECG-Acquisition IC with Analog Feature Extraction **3:15 PM**
L. Yan[1], P. Harpe[2], M. Osawa[3], Y. Harada[3], K. Tamiya[3], C. van Hoof[1,4], R. F. Yazicioglu[1]
[1]imec, Heverlee, Belgium
[2]Eindhoven University of Technology, Eindhoven, The Netherlands
[3]Olympus, Tokyo, Japan; [4]KU Leuven, Leuven, Belgium

24.5 A 0.5V 1.27mW Nose-on-a-Chip for Rapid Diagnosis of Ventilator-Associated Pneumonia **3:45 PM**
K-T. Tang[1], S-W. Chiu[1], C-H. Shih[2], C-L. Chang[1], C-M. Yang[1], D-J. Yao[1], J-H. Wang[1], C-M. Huang[1], H. Chen[1], K-H. Chang[1], C-C. Hsieh[1], T-H. Chang[1], M-F. Chang[1], C-M. Wang[1], Y-W. Liu[1], T-J. Chen[3], C-H. Yang[3], H. Chiueh[3], J-M. Shyu[1]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Taipei Medical University, Taipei, Taiwan
[3]National Chiao Tung University, Hsinchu, Taiwan

24.6 A CMOS Micro-Flow Cytometer for Magnetic Label Detection and Classification **4:15 PM**
P. Murali, I. Izyumin, D. Cohen, J-C. Chien, A. M. Niknejad, B. Boser
University of California, Berkeley, CA

24.7 A 60nV/√Hz 15-Channel Digital Active Electrode System for Portable Biopotential Signal Acquisition **4:30 PM**
J. Xu[1,2], B. Busze[1], H. Kim[3], K. Makinwa[2], C. van Hoof[3], R. F. Yazicioglu[1,3]
[1]Holst Centre/imec, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
[3]Holst Centre/imec, Leuven, Belgium

24.8 An Analog-Digital-Hybrid Single-Chip RX Beamformer with Non-Uniform Sampling for 2D-CMUT Ultrasound Imaging to Achieve Wide Dynamic Range of Delay and Small Chip Area **4:45 PM**
J-Y. Um[1], E-W. Song[1], Y-J. Kim[1], S-E. Cho[1], M-K. Chae[1], J. Song[2], B. Kim[2], S. Lee[2], J. Bang[2], Y. Kim[2], K. Cho[2], B. Kim[1], J-Y. Sim[1], H-J. Park[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Advanced Institute of Technology, Yongin, Korea

Conclusion **5:15 PM**

High-Bandwidth Low-Power DRAM and I/O

Session Chair: Uksong Kang, *Samsung Electronics, Hwasung, Korea*
Associate Chair: James Sung, *Etron Technology, Hsinchu, Taiwan*

25.1 A 3.2Gb/s/pin 8Gb 1.0V LPDDR4 SDRAM with Integrated ECC Engine for Sub-1V DRAM Core Operation **1:30 PM**

T-Y. Oh, H. Chung, Y-C. Cho, J-W. Ryu, K. Lee, C. Lee, J-I. Lee, H-J. Kim, M. S. Jang, G-H. Han, K. Kim, D. Moon, S. Bae, J-Y. Park, K-S. Ha, J. Lee, S-Y. Doo, J-B. Shin, C-H. Shin, K. Oh, D. Hwang, T. Jang, C. Park, K. Park, J-B. Lee, J. S. Choi
Samsung Electronics, Hwasung, Korea

25.2 A 1.2V 8Gb 8-Channel 128GB/s High-Bandwidth Memory (HBM) Stacked DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV **2:00 PM**

D. U. Lee, K. W. Kim, K. W. Kim, H. Kim, J. Y. Kim, Y. J. Park, J. H. Kim, D. S. Kim, H. B. Park, J. W. Shin, J. H. Cho, K. H. Kwon, M. J. Kim, J. Lee, K. W. Park, B. Chung, S. Hong
SK Hynix, Icheon, Korea

25.3 A 1.35V 5.0Gb/s/pin GDDR5M with 5.4mW Standby Power and an Error-Adaptive Duty-Cycle Corrector **2:30 PM**

H-W. Lee[1,2], J. Song[2], S-A. Hyun[1], S. Baek[1], Y. Lim[1], J. Lee[1], M. Park[1], H. Choi[1], C. Choi[1], J. Cha[1], J. Kim[1], H. Choi[1], S. Kwack[1], Y. Kang[1], J. Kim[1], J. Park[1], J. Kim[1], J. Cho[1], C. Kim[2], Y. Kim[1], J. Lee[1], B. Chung[1], S. Hong[1]
[1]SK Hynix, Icheon, Korea
[2]Korea University, Seoul, Korea

Break **3:00 PM**

Energy-Efficient Dense Interconnect

Session Chair: SeongHwan Cho, *KAIST, Daejeon, Korea*
Associate Chair: Hisakatsu Yamaguchi, *Fujitsu Laboratories, Kawasaki, Japan*

26.1 A 130mW 20Gb/s Half-Duplex Serial Link in 28nm CMOS **3:15 PM**
V. Balan, O. Oluwole, G. Kodani, C. Zhong, S. Maheswari, R. Dadi, A. Amin, G. Bhatia, P. Mills, A. Ragab, E. Lee
nVidia, Santa Clara, CA

26.2 A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS DS **3:45 PM**
J. Jaussi[1], G. Balamurugan[1], S. Hyvonen[1], T-C. Hsueh[1], T. Musah[1], G. Keskin[1], S. Shekhar[1], J. Kennedy[1], S. Sen[1], R. Inti[1], M. Mansuri[1], M. Leddige[1], B. Horine[1], C. Roberts[1], R. Mooney[2], B. Casper[1]
[1]Intel, Hillsboro, OR
[2]Intel, Mapleton, UT

26.3 A Pin- and Power-Efficient Low-Latency 8-to-12Gb/s/wire 8b8w-Coded SerDes Link for High-Loss Channels in 40nm Technology DS **4:15 PM**
A. Singh[1], D. Carnelli[1], A. Falay[1], K. Hofstra[1], F. Licciardello[1], K. Salimi[1], H. Santos[1], A. Shokrollahi[1], R. Ullrich[1], C. Walter[1], J. Fox[2], P. Hunt[2], R. Simpson[2], A. Stewart[2], G. Surace[2]
[1]Kandou Bus, Lausanne, Switzerland
[2]Kandou Bus, Northampton, United Kingdom

26.4 A 25.6Gb/s Differential and DDR4/GDDR5 Dual-Mode Transmitter with Digital Clock Calibration in 22nm CMOS **4:45 PM**
T-C. Hsueh, G. Balamurugan, *J. Jaussi, S. Hyvonen, J. Kennedy, G. Keskin, T. Musah, S. Shekhar*, R. Inti, S. Sen, M. Mansuri, C. Roberts, B. Casper*
Intel, Hillsboro, OR
*now at University of British Columbia, Vancouver, BC, Canada

26.5 An 8-to-16Gb/s 0.65-to-1.05pJ/b 2-Tap Impedance-Modulated Voltage-Mode Transmitter with Fast Power-State Transitioning in 65nm CMOS **5:00 PM**
Y-H. Song[1], H-W. Yang[1], H. Li[2], P. Y. Chiang[2,3], S. Palermo[1]
[1]Texas A&M University, College Station, TX
[2]Oregon State University, Corvallis, OR
[3]Fudan University, Shanghai, China

26.6 A 2.667Gb/s DDR3 Memory Interface with Asymmetric ODT on Wirebond Package and Single-Side-Mounted PCB **5:15 PM**
S-P. Chen, C-C. Hung, Q-T. Chen, S-M. Chang, M-S. Liou, B-W. Hsieh, H-I. Huang, B. Liu, Y-B. Luo
MediaTek, Hsinchu, Taiwan

Conclusion **5:30 PM**

Energy-Efficient Digital Circuits

Session Chair: Bing Sheu, *TSMC, Hsinchu, Taiwan*
Associate Chair: Marian Verhelst, *KU Leuven, Heverlee, Belgium*

27.1 A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, Embedding F_{MAX} Tracking — **1:30 PM**
R. Wilson[1], E. Beigne[2], P. Flatresse[1], A. Valentian[2], F. Abouzeid[1], T. Benoist[2], C. Bernard[2], S. Bernard[2], O. Billoint[2], S. Clerc[1], B. Giraud[2], A. Grover[1], J. Le Coz[1], I. Miro Panades[2], J-P. Noel[1], B. Pelloux-Prayer[1], P. Roche[1], O. Thomas[2], Y. Thonnart[2], D. Turgis[1], F. Clermidy[2], P. Magarshack[1]
[1]STMicroelectronics, Crolles, France
[2]CEA-LETI - MINATEC, Grenoble, France

27.2 A 6mW 5K-Word Real-Time Speech Recognizer Using WFST Models — **2:00 PM**
M. Price, J. Glass, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

27.3 A 210mV 5MHz Variation-Resilient Near-Threshold JPEG Encoder in 40nm CMOS — **2:30 PM**
N. Reynders, W. Dehaene
KU Leuven, Leuven, Belgium

Break — **3:00 PM**

27.4 A 0.75-Million-Point Fourier-Transform Chip for Frequency-Sparse Signals — **3:15 PM**
O. Abari, E. Hamed, H. Hassanieh, A. Agarwal, D. Katabi, A. P. Chandrakasan, V. Stojanovic
Massachusetts Institute of Technology, Cambridge, MA

27.5 A Multi-Granularity FPGA with Hierarchical Interconnects for Efficient and Flexible Mobile Computing — **3:45 PM**
C. C. Wang[1], F-L. Yuan[1], T-H. Yu[2], D. Markovic[1]
[1]University of California, Los Angeles, CA
[2]Qualcomm, Irvine, CA

27.6 An 821MHz 7.9Gb/s 7.3pJ/b/iteration Charge-Recovery LDPC Decoder — **4:15 PM**
T-C. Ou, Z. Zhang, M. C. Papaefthymiou
University of Michigan, Ann Arbor, MI

27.7 A Scalable 1.5-to-6Gb/s 6.2-to-38.1mW LDPC Decoder for 60GHz Wireless Networks in 28nm UTBB FDSOI — **4:45 PM**
M. Weiner[1], M. Blagojevic[1,2,3], S. Skotnikov[4], A. Burg[4], P. Flatresse[3], B. Nikolic[1]
[1]University of California, Berkeley, CA
[2]Institute Supérieur d'Electronique de Paris, Paris, France
[3]STMicroelectronics, Crolles, France
[4]EPFL, Lausanne, Switzerland

27.8 A Static Contention-Free Single-Phase-Clocked 24T Flip-Flop in 45nm for Low-Power Applications — **5:00 PM**
Y. Kim, W. Jung, I. Lee, Q. Dong, M. Henry, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

Conclusion — **5:15 PM**

SESSION 28 Wednesday February 12th, 1:30 PM

Mixed-Signal Techniques for Wireless

Session Chair: Shouhei Kousai, Toshiba, Kawasaki, Japan
Associate Chair: Jan van Sinderen, *NXP Semiconductors, Eindhoven, The Netherlands*

28.1 A Programmable 0.7-to-2.7GHz Direct ΔΣ Receiver in 40nm CMOS **1:30 PM**
M. Englund[1], K. B. Östman[1], O. Viitala[1], M. Kaltiokallio[1], K. Stadius[1], K. Koli[2], J. Ryynänen[1]
[1]Aalto University, Espoo, Finland
[2]Ericsson, Turku, Finland

28.2 A 0.29mm² Frequency Synthesizer in 40nm CMOS with 0.19ps$_{rms}$ Jitter and <-100dBc Reference Spur for 802.11ac **2:00 PM**
Y-L. Hsueh, L-C. Cho, C-H. Shen, Y-C. Tsai, T-C. Chueh, T-Y. Chang, J-L. Hsu, J-H. C. Zhan
MediaTek, Hsinchu, Taiwan

28.3 A Frequency-Defined Vernier Digital-to-Time Converter for Impulse Radar Systems in 65nm CMOS **2:30 PM**
Y-H. Kao, C-M. Lai, J-M. Wu, P-C. Huang, P-H. Hsieh, T-S. Chu
National Tsing Hua University, Hsinchu, Taiwan

Break **3:00 PM**

SESSION 29 Wednesday February 12th, 3:15 PM

Data Converters for Wireless Systems

Session Chair: Gerhard Mitteregger, *Intel Mobile Communications, Taufkirchen, Germany*
Associate Chair: Brian Brandt, *Maxim Integrated, North Chelmsford, MA*

29.1 A 5mW CT ΔΣ ADC with Embedded 2nd-Order Active Filter and VGA Achieving 82dB DR in 2MHz BW **3:15 PM**
R. Rajan, S. Pavan
IIT Madras, Chennai, India

29.2 A 235mW CT 0-3 MASH ADC Achieving -167dBFS/Hz NSD with 53MHz BW **3:45 PM**
Y. Dong[1], R. Schreier[1], W. Yang[2], S. Korrapati[2], A. Sheikholeslami[1,3]
[1]Analog Devices, Toronto, ON, Canada
[2]Analog Devices, Wilmington, MA
[3]University of Toronto, Toronto, ON, Canada

29.3 A 14b 1GS/s RF Sampling Pipelined ADC with Background Calibration **4:15 PM**
A. M. Ali[1], H. Dinc[1], P. Bhoraskar[1], C. Dillon[1], S. Puckett[1], B. Gray[1], C. Speir[1], J. Lanford[1], D. Jarman[1], J. Brunsilius[2], P. Derounian[1], B. Jeffries[1], U. Mehta[1], M. McShea[1], H-Y. Lee[3]
[1]Analog Devices, Greensboro, NC
[2]Analog Devices, San Diego, CA
[3]Analog Devices, Wilmington, MA

Conclusion **4:45 PM**

Technologies for Next-Generation Systems

Session Chair: Fu-Lung Hsueh, *TSMC, Hsinchu, Taiwan*
Associate Chair: Jan Genoe, *imec, Leuven, Belgium*

30.1 8-bit Thin-Film Microprocessor Using a Hybrid Oxide-Organic Complementary Technology with Inkjet-Printed P²ROM Memory — 1:30 PM

K. Myny[1], S. Smout[1], M. Rockelé[1,2], A. Bhoolokam[1,2], T. H. Ke[1], S. Steudel[1], K. Obata[3], M. Marinkovic[4], D-V. Pham[4], A. Hoppe[4], A. Gulati[5], F. Gonzalez Rodriguez[5], B. Cobb[5], G. H. Gelinck[5], J. Genoe[1,2], W. Dehaene[1,2], P. Heremans[1,2]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium; [3]Panasonic, Osaka, Japan; [4]Evonik Industries, Marl, Germany; [5]Holst Centre/TNO, Eindhoven, The Netherlands

30.2 Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption — DS — 2:00 PM

J. Genoe[1,2], K. Obata[3], M. Ameys[1], K. Myny[1], T. H. Ke[1], M. Nag[1], S. Steudel[1], S. Schols[1], J. Maas[4], A. Tripathi[4], J-L. van der Steen[4], T. Ellis[4], G. H. Gelinck[4], P. Heremans[1,2,4]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium
[3]Panasonic, Osaka, Japan; [4]Holst Centre/TNO, Eindhoven, The Netherlands

30.3 Organic-Transistor-Based 2kV ESD-Tolerant Flexible Wet Sensor Sheet for Biomedical Applications with Wireless Power and Data Transmission Using 13.56MHz Magnetic Resonance — 2:30 PM

H. Fuketa[1,2], K. Yoshioka[1,2], T. Yokota[1,2], W. Yukita[1,2], M. Koizumi[1,2], M. Sekino[1,2], T. Sekitani[1,2], M. Takamiya[1,2], T. Someya[1,2], T. Sakurai[1,2]
[1]University of Tokyo, Tokyo, Japan; [2]JST/ERATO, Tokyo, Japan

30.4 A 13.56MHz RFID Tag with Active Envelope Detection in an Organic Complementary TFT Technology — 2:45 PM

V. Fiore[1], E. Ragonese[2], S. Abdinia[3], S. Jacob[4], I. Chartier[4], R. Coppard[4], A. van Roermund[3], E. Cantatore[3], G. Palmisano[1]
[1]University of Catania, Catania, Italy; [2]STMicroelectronics, Catania, Italy
[3]Eindhoven University of Technology, Eindhoven, The Netherlands
[4]CEA-LITEN, Grenoble, France

Break — 3:00 PM

30.5 A GaN 3×3 Matrix Converter Chipset with Drive-by-Microwave Technologies — 3:15 PM

S. Nagai[1], Y. Yamada[1], N. Negoro[2], H. Handa[2], Y. Kudoh[1], H. Ueno[1], M. Ishida[2], N. Otuska[1], D. Ueda[1]
[1]Panasonic, Osaka, Japan; [2]Panasonic, Kyoto, Japan

30.6 An Electromagnetic Clip Connector for In-Vehicle LAN to Reduce Wire Harness Weight by 30% — 3:45 PM

A. Kosuge, S. Ishizuka, L. Liu, A. Okada, M. Taguchi, H. Ishikuro, T. Kuroda
Keio University, Yokohama, Japan

30.7 A 60Mb/s Wideband BCC Transceiver with 150pJ/b RX and 31pJ/b TX for Emerging Wearable Applications — 4:00 PM

J. Lee[1], V. V. Kulkarni[1], C. K. Ho[1], J. H. Cheong[1], P. Li[1], J. Zhou[1], W. D. Toh[1], X. Zhang[1], Y. Gao[1], K. W. Cheng[2], X. Liu[1], M. Je[1]
[1]Institute of Microelectronics, Singapore, Singapore
[2]National Cheng Kung University, Tainan, Taiwan

30.8 A 30GS/s Double-Switching Track-and-Hold Amplifier with 19dBm IIP3 in an InP BiCMOS Technology — 4:15 PM

T. D. Gathman[1,2], K. N. Madsen[2,3], J. C. Li[4], T. C. Oh[4], J. F. Buckwalter[2]
[1]Qualcomm, San Diego, CA; [2]University of California, San Diego, La Jolla, CA
[3]Peregrine Semiconductor, San Diego, CA; [4]HRL Laboratories, Malibu, CA

30.9 Normally-Off Computing with Crystalline InGaZnO-based FPGA — 4:30 PM

T. Aoki[1], Y. Okamoto[1], T. Nakagawa[1], M. Ikeda[1], M. Kozuma[1], T. Osada[1], Y. Kurokawa[1], T. Ikeda[1], N. Yamade[1], Y. Okazaki[1], H. Miyairi[1], M. Fujita[2], J. Koyama[1], S. Yamazaki[1]
[1]Semiconductor Energy Laboratory, Kanagawa, Japan; [2]University of Tokyo, Tokyo, Japan

30.10 A 1TOPS/W Analog Deep Machine-Learning Engine with Floating-Gate Storage in 0.13μm CMOS — 4:45 PM

J. Lu, S. Young, I. Arel, J. Holleman; University of Tennessee, Knoxville, TN

Conclusion — 5:15 PM

Short Course: Biomedical and Sensor Interface Circuits

Chair: ***Willy Sansen,*** *KU Leuven, Belgium*

An increasing number of circuits interface with the human body and other bio-sensors. They have to interface with living tissues, which change in impedance, with temperature, and with time. Very high input circuit impedances are required to avoid the extraction of current, causing drift and infection. High sensitivity and low noise are required as well.

This short course aims to describe the difficulties and technical solutions for such bio-interface circuits. Successful realizations are presented for different kinds of medical applications.

The Biomedical Electrode-Tissue Interface: A Simple Explanation of a Complex Subject

Eric McAdams, I*NAS, Lyon, France*

Biomedical electrodes are used in various forms in a wide range of biomedical applications. Good electrode design is not as simple as is often assumed, and all electrode designs are not equal in performance. One must not simply choose an electrode with as conductive a sensing element as possible, which unfortunately, was and still is the case in many designs, especially in the emerging area of "wearable sensing".

Monitoring bioelectrodes, if they are not chosen/designed correctly, give rise to significant problems that make biosignal analysis difficult, if not impossible. Both the electrode–electrolyte interface and the skin under the electrode (collectively known as the contact) give rise to potentials and impedances that can distort the measured biosignal. The potentials and impedances of the electrode–electrolyte interface and of the skin will therefore be studied in some depth using a simple yet effective model to give a sound working knowledge of biomedical electrode technology and design.

About the presenter:
Prof. Eric McAdams is Head of the Medical Sensors Group within INL and works and teaches at INSA Lyon. Before that he was Head of the Medical Sensors Group at NIBEC, University of Ulster, and he co-founded and was a director of a successful spin-off company, Intelesens. Intelesens researches, designs, develops, and manufactures innovative, devices in pioneering areas such as wireless Vital Signs Monitoring. He is widely recognized as a leading specialist in the study and modeling of the electrical properties of materials and interfaces. He has successfully designed, developed, patented and commercialized a wide range of Biomedical Sensors and Electrodes.

Low-Power Interface Circuits for Bio-Potential and Physiological Signal Acquisition

Firat Yazicioglu, *IMEC, Leuven, Belgium*

With an increasing number of applications, smarter and smaller wearable/implantable biomedical devices have been one of the main drivers behind low-power analog IC design for sensor interfaces. In recent years, the adoption of wearable devices for wellness applications has boosted the need for such sensor interfaces making them even more interesting for the research community and industry.

This presentation focuses on the instrumentation amplifiers and readout circuits for the readout of different biomedical signal modalities. The course starts with minimum safety and performance requirements for different applications. Later, signal integrity problems are discussed and circuit and environmental noise sources are introduced. A large part of course is on the design of sensor interface circuits and instrumentation amplifiers for different signal modalities that are relevant for both wearable and implantable applications such as bio-potential, bio-impedance, and optical measurements. Finally, commercially available ICs in the field are introduced and future directions are discussed.

About the presenter:
Firat Yazicioglu received the Ph.D. degree in Electrical Eng. from Katholieke Universiteit Leuven in 2008. He is currently at IMEC, Belgium where he leads the "Biomedical Integrated Circuits" team focusing on Mixed Signal Integrated Circuit design for wearable and implantable bio-

medical applications. He has (co)authored over 70 publications and several patents in the field of IC design for biomedical applications. He has contributed/lead the development of several generations of integrated circuits for wearable and implantable healthcare applications, some of which are absorbed by the industry for commercialization. Dr. Yazicioglu serves on the technical program committees of ESSCIRC and ISSCC. He is the co-chair of BioCAS 2013.

Design Strategies for Wearable Sensor Interface Circuits - from Electrodes to Signal Processing

Jerald Yoo, *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

Wearable healthcare sensors provide attractive opportunities for the semiconductor sector. The target is to mitigate the impact of chronic diseases by providing continuous yet adequate low-noise *monitoring and analysis* of physiological signals. The wearable environment is challenging for circuit designers due to its unstable skin-electrode interface. Wet and dry electrodes have very different electrical characteristics that need to be addressed. Also, in a wearable environment, a trade-off between available resources and component performance (analog front-end and digital back-end) is crucial.

This short course covers the design strategies for bio-interface circuits for such wearable sensors. We first explore the difficulties, limitations and potential pitfalls in wearable interfaces, and strategies to overcome them. After that, system-level considerations for better key metrics such as energy efficiency are introduced. Several state-of-the-art instrumentation amplifiers that emphasize different parameters are also discussed. We then see how the signal analysis part impacts the analog interface circuit design. The talk concludes with interesting aspects and opportunities that lie ahead.

About the presenter:
Jerald Yoo received the Ph.D. degree in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2010. In May 2010, he joined the Faculty of Microsystems Engineering, Masdar Institute, Abu Dhabi, United Arab Emirates, where he is an Assistant Professor. Dr. Yoo developed low-energy Body Area Network (BAN) transceivers and wearable body sensor networks using Planar-Fashionable Circuit Board (P-FCB) for continuous health monitoring. His research focuses on low-energy circuit technology for wearable bio signal sensors, wireless power transmission, SoC design to system realization for wearable healthcare applications, and energy-efficient biomedical circuit techniques. He is an author of a book chapter in Biomedical CMOS ICs (Springer, 2010). Dr. Yoo is a co-recipient of the Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards in 2005.

System Architectures and Strategies for Bi-directional Interfacing of Circuits with Physiological Systems

Tim Denison, *Medtronic, Minneapolis, MN*

This talk presents state-of-the-art circuit techniques for *bi-directionally* interfacing to physiological systems with the goal of restoring function. To provide context for the design discussion, a general framework of sensors, classifiers, control policies and actuators is first covered. The circuit design constraints and implementations for each of these sub-blocks is then discussed, along with the relevant physiological principles that guide the overall design. Examples of how the sub-systems are integrated together with physiology are then drawn from cardiac, neural, and prosthetic system applications. To close the discussion, a commentary on potential future trends is given.

About the presenter:
Tim Denison is a Technical Fellow at Medtronic and Director of Core Technology in the Neuromodulation division, where he helps oversee the design of next generation neural interface and algorithm technologies for the treatment of chronic neurologic disease. In 2012, he was awarded membership to the Bakken Society, Medtronic's highest technical and scientific honor. Tens of thousands of patients receive implantable circuits each year from systems Tim helped design. He received a Ph.D. in Electrical Engineering from MIT. He is also a graduate of Harvard Business School's Program for Leadership Development. Tim's extracurricular pursuits include serving as an Adjunct Assistant Professor at Brown University, teaching "smart" medical sensor design short courses at TU Delft, and chairing the IEEE EMBS society Twin Cities chapter.

F3: Adaptive Design Techniques for Energy Efficiency

Organizer: Eric Fluhr, *IBM, Austin, TX*

Committee:

Eric Fluhr, *IBM, Austin, TX*
Michael Polley, *Samsung Mobile, Dallas, TX*
Se-Hyun Yang, *Samsung, Yongin-Si, Korea*
Vasantha Erraguntla, *Intel, Bangalore, India*
Tobias Noll, RWTH Aachen *University, Aachen, Germany*
Kees van Berkel, *Ericsson, Eindhoven, The Netherlands*

Silicon technology continues to shrink, allowing a greater density of devices per unit area. At the same time, process and chip variations increase, making it more difficult to build power-efficient, functional chips. We first review the physical issues that are driving such increasing variation. Then, we look at state-of-the-art approaches to adapt to this variation. Voltage management is a key element, both in innovative management circuits, as well as in integration across the hardware/software design stack for adaptive control of the system. Leveraging error tolerance, where available, is as critical as building new memories that can avoid or mitigate sensitivity to variation. Finally, innovative models to predict the effects of variations are critical to guiding choices in the design process.

Agenda

Time	Topic
8:00	Breakfast
8:20	Introduction by the Chair
8:30	**Process Technology Variation Characteristics and Trends** ***Martin Giles,*** *Intel*, *Hillboro, OR*
9:15	**Robust and Resilient Systems from the Bottom-Up: Circuits, Architecture and Software Integration** ***Vijay Reddi,*** *University of Texas, Austin, TX*
10:00	Break (15 min)
10:15	**Ultra-Low Power Computing Systems with Graceful Performance Degradation on Unreliable Silicon** ***Andreas Burg,*** *EPFL, Lausanne, Switzerland*
11:00	**Enabling Adaptive Techniques in High-Volume Design** ***Sam Naffziger,*** *AMD, Fort Colins, CO*
11:45	Lunch
13:00	**Design of Adaptive and Resilient Circuits for Power-Delivery Solutions** ***Ramnarayanan Muthukaruppan,*** *Intel, Bengaluru, India*
13:45	**Variability and Design of SRAM in Nanoscale CMOS and Emerging Device Technologies** ***Ching-te Chuang,*** *National Chiao-Tung University, Hsinchu, Taiwan*
14:30	Break
14:45	**Predictive Simulation of Performance and Variability at and Beyond 14nm and Impact on Design** ***Asen Asenov,*** *University of Glasgow, Glasgow, United Kingdom*
15:30	Optional: panel discussion (20 min)
15:50	Closing remarks by the Chair

F4: mm-Wave Advances for Active Safety and Communication Systems

Organizer: Marc Tiebout, *Infineon Technologies, Villach, Austria*

Committee:

Brian Floyd, *North Carolina State University, Raleigh, NC*
Mike Keaveney, *Analog Devices, Limerick, Ireland*
Marc Tiebout, *Infineon Technologies, Villach, Austria*
Pierre Busson, *STMicroelectronics, Crolles, France*
Kenichi Okada, *Tokyo Institute of Technology, Tokyo, Japan*

Recent advances in microwave and mm-Wave applications targeting existing and upcoming safety, radar and communication systems will be presented. Speakers from university and major industry companies will highlight both system aspects as well as implementation aspects, including packaging and high-volume production testing. Topics include car-to-car / car-to-x communications, FMCW and pulse radar, MIMO and novel CMOS-based architectures. Silicon implementations for frequencies from 5GHz to 240GHz in SiGe and CMOS will be presented. Emphasis is placed on automotive 77-to-79GHz radar, which is the highest-volume existing mm-Wave application.

Agenda

Time	Topic
8:00	Breakfast
8:30	Introduction by Chair
8:40	**Wireless Transceivers for Car2Car & Car2X Systems and Applications** ***Marc Klaassen,*** *BU Automotive - Car Entertainment Solutions, NXP Semiconductors, Nijmegen, The Netherlands*
9:25	**Current and Future Application Requirements of mm-Wave Radar Sensors** ***Nils Pohl,*** *Fraunhofer FHR, Wachtberg, Germany*
10:20	Break
10:35	**Packaging Technologies and Production Test for Automotive Radar Front-End Products, *Sergio Pacheco,*** *Freescale Semiconductors, Phoenix, AZ*
11:25	**CMOS Realization of 24/26/77/79 GHz FMCW and Pulse Radars for Automotive Applications, *Jri Lee,*** *National Taiwan University, Taipei, Taiwan*
12:15	Lunch
13:30	**Applications and Implementations of Integrated Direct-Sampling Impulse Radar Systems, *T.-S. Chu,*** *National Tsing Hua University, Hsinchu, Taiwan*
14:20	**Millimeter-Wave MIMO Radar in CMOS for Vehicular Applications** ***Harish Krishnaswamy,*** *Columbia University, New York, NY*
15:10	Break
15:25	**24GHz Versus 79GHz Automotive Radar Sensors, Applications and Implementations, *Patrice Garcia,*** *STMicroelectronics, Crolles, France*
16:15	Closing remarks by Chair

F5: Low-Power Radios for Sensor Networks

Organizer: **Woogeun Rhee,** *Tsinghua University, Beijing, China*

Chair: **Gangadhar Burra,** *Qualcomm-Atheros, San Jose, CA*

Committee: **Kazutami Arimoto,** *Okayama Prefectural University, Okayama, Japan*
Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*
Brian Otis, *University of Washington, Seattle, CA*
David Ruffieux, *CSEM, Neuchatel, Switzerland*

Sensor node systems are expected to be a major growth field for semiconductor markets, and will connect to the cloud in a future cyber physical world. Wireless sensor networks (WSN) face multiple challenges from system design to low-power electronics and energy sources. Ultra-low-power radios are key elements in such systems, putting high demand on energy efficiency in different modes of operation (active, wake-up and sleep). This forum presents system perspectives and practical design aspects in various energy-efficient and short-range radio circuits and systems, including an introduction to various applications and their requirements for RF and digital signal processing in WSN systems. The technologies range from RF to digital signal processing and algorithms to give comprehensive understanding of recent advances. The forum begins with two high-level design talks on low power radio SoCs. The following four talks present ultra-low-power transceivers for body-area networks, sensor nodes, and health-monitoring applications. The last two talks cover efficient power management and emerging compression methodologies.

Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** ***Gangadhar Burra,*** *Qualcomm-Atheros, San Jose, CA*
8:30	**Wireless Medical Device Communication: Performance Considerations, System Design, and Recent Innovations** ***Peter Bradley,*** *Microsemi, Sydney, Australia*
9:20	**Low-Power Radio SoCs and Microsystems for Tiny-Battery-Operated Healthcare and Lifestyle Applications** ***Vincent Peiris,*** *CSEM, Neuchatel, Switzerland*
10:10	Break
10:35	**Multistandard Transceiver and SoC Design for WBAN** ***Alan Wong,*** *Toumaz Microsystems, Abingdon, United Kingdom*
11:25	**Wireless Communication for Cubic-mm Sensor Nodes** ***David D. Wentzloff,*** *University of Michigan, Ann Arbor, MI*
12:15	Lunch
13:20	**CMOS Radios for Health Monitoring: Closing the Gap between Power and Performance** ***Jagdish Pandey,*** *Qualcomm, San Diego, CA*
14:10	**Challenges in ULP Event-Driven Transceiver Design** ***Guido Dolmans,*** *imec - Holst Centre, Eindhoven, The Netherlands*
15:00	Break
15:20	**Normally-Off Computing for Sensor-Net Applications** ***Hiroshi Nakamura,*** *University of Tokyo, Tokyo, Japan*
16:10	**Mixed-Signal Processing for Low-Power WSN/BAN** ***Hyejung Kim,*** *imec, Heverlee, Belgium*
17:00	Closing Remarks (Chair)

F6: Energy-Efficient I/O Design for Next-Generation Systems

Organizer: **Frank O'Mahony,** *Intel, Hillsboro, OR*

Committee:

Nicola da Dalt, *Infineon, Villach, Austria*
Ken Chang, *Xilinx, San Jose, CA*
Hisakatsu Yamaguchi, *Fujitsu, Kawasaki, Japan*
Chulwoo Kim, *Korea University, Seoul, Korea*
Elad Alon, *University of California Berkeley, Berkeley, CA*

System power consumption will drive the architecture of future computing systems. From cloud-connected smart phones to the first exaFLOP supercomputers, systems that are the best at managing and minimizing power consumption will hold a key competitive advantage. At the same time, wireline communication bandwidth requirements within these systems will continue to grow exponentially, driving per-lane data rates beyond 25Gb/s and aggregate bandwidth past 1Tb/s while demanding dramatically improved energy efficiency. The objective of this Forum is to provide an overview of ultra-efficient parallel and serial interfaces, advanced memory applications, dense and high-speed optical communication, and platform-driven wired I/O for mobile. The Forum begins with two talks describing how innovative packaging and form factors along with co-design of I/O circuits and interconnects can improve the power/performance tradeoff by more than an order of magnitude. The next two talks address how memory I/O is adapting to meet the aggressive bandwidth and power requirements for systems ranging from cell phones to supercomputers. The next talk explores how to design serial I/O specifically for mobile products, including low-power equalization and clocking and low-latency standby states. The following talk also focuses on energy-efficient clocking and equalization, but explores analog and digital design options for very high-speed link standards. The final two talks highlight recent advances in both discrete and integrated optical transceivers and the power, performance, density and cost benefits for optical in high-performance computing systems.

Agenda

Time	Topic
8:00	Breakfast
8:20	Introduction by Chair
8:30	**Advanced Packaging for Low-Power I/O** ***Liam Madden,*** *Xilinx, San Jose, CA*
9:20	**Co-Designing Channel, Signal, and Circuits for High-Bandwidth Low-Power I/O,** ***John Poulton,*** *NVIDIA, Durham, NC*
10:10	Break (15 min)
10:35	**Low-Power Memory for Mobile,** ***Hyun-Woo Lee,*** *SK Hynix, Ichon, Korea*
11:25	**Enabling the Next 10× Leap in Memory Bandwidth** ***Feng Lin,*** *Micron, Boise, ID*
12:15	Lunch
13:20	**Ultra-Efficient Mobile I/O,** ***James Jaussi,*** *Intel, Hillsboro, OR*
14:10	**Low-Power Equalization and CDR for 10-to-28Gb/s SerDes** ***Thomas Toifl,*** *IBM, Ruschlikon, Switzerland*
15:00	Break
15:20	**Energy-Efficient 25Gb/s Optical Transceivers** ***Takashi Takemoto,*** *Hitachi, Tokyo, Japan*
16:10	**Low-Power Si Photonics for Ultra-Dense Optical I/O** ***Brian Welch,*** *Luxtera, Carlsbad, CA*
17:00	Closing remarks by Chair

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

EXECUTIVE COMMITTEE

CONFERENCE CHAIR
Anantha Chandrakasan, *Massachusetts Institute of Technology, Cambridge, MA*

SECRETARY, PRESS COORDINATOR AND DATA TEAM CHAIR
Siva Narendra, *Tyfone, Portland, OR*

DIRECTOR OF FINANCE AND BOOK DISPLAY COORDINATOR
Bryant Griffin, *Penfield, NY*

PROGRAM CHAIR
Trudy Stetzler, *Halliburton, Houston, TX*

PROGRAM VICE CHAIR
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*

STUDENT RESEARCH CHAIR AND UNIVERSITY RECEPTIONS
Jan Van der Spiegel, *University of Pennsylvania, Philadelphia, PA*

DEMONSTRATION SESSION CO- CHAIR
Bill Bowhill, *Intel, Hudson, MA*

DEMONSTRATION SESSION CO-CHAIR
Uming Ko, *MediaTek, Austin, TX*

ITPC FAR EAST REGIONAL CHAIR
Kazutami Arimoto, *Okayama Prefectural University, Okayama, Japan*

ITPC FAR EAST REGIONAL VICE CHAIR
Jae-Youl Lee, *Samsung, Yongin, Korea*

ITPC FAR EAST REGIONAL SECRETARY
Tsung-Hsien Lin, *National Taiwan University, Taipei, Taiwan*

ITPC EUROPEAN REGIONAL CHAIR
Alison Burdett, *Toumaz Microsystems, Abingdon, United Kingdom*

ITPC EUROPEAN REGIONAL VICE CHAIR AND SECRETARY
Maurits Ortmanns, *University of Ulm, Ulm Germany*

ADCOM REPRESENTATIVE
Bryan Ackland, *Stevens Institute of Technology, Old Bridge, NJ*

DIRECTOR OF PUBLICATIONS AND PRESENTATIONS
Laura Fujino, *University of Toronto, Toronto, Canada*

DIRECTOR OF AUDIOVISUAL SERVICES
John Trnka, *Rochester, MN*

PRESS LIAISON AND AWARDS & RECOGNITION COMMITTEE (ARC) CHAIR
Kenneth C. Smith, *University of Toronto, Toronto, Canada*

FORUMS CHAIR
Bram Nauta, *University of Twente, Enschede, The Netherlands*

EDUCATIONAL EVENTS CHAIR
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*

DIRECTOR OF OPERATIONS
Melissa Widerkehr, *Widerkehr and Associates, Montgomery Village, MD*

TECHNICAL EDITORS

Jason H. Anderson, *University of Toronto, Toronto, Canada*
Dustin Dunwell (*Editor-at-Large)*, *Kapik Integration, Toronto, Canada*
Vincent Gaudet, *University of Waterloo, Waterloo, Canada*
Glenn Gulak *(Editor-at-Large)*, *University of Toronto, Toronto, Canada*
James W. Haslett, *University of Calgary, Calgary, Canada*
Shahriar Mirabbasi, *(Editor-at-Large)* *University of British Columbia, Vancouver, Canada*
Kostas Pagiamtzis, *Semtech, Gennum Products Group, Burlington, Canada*
Kenneth C. Smith *(Editor-at-Large)*, *University of Toronto, Toronto, Canada*

MULTI-MEDIA COORDINATOR

Dave Halupka, *Kapik Integration, Toronto, Canada*

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

PROGRAM CHAIR:
Trudy Stetzler, Halliburton, Houston, TX

PROGRAM VICE CHAIR:
Hoi-Jun Yoo, KAIST, Daejeon, Korea

ANALOG SUBCOMMITTEE

Chair: Axel Thomsen, Silicon Laboratories, Austin, TX
Anton Bakker, IDT, Morgan Hill, CA
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Minkyu Je, Institute of Microelectronics, A*STAR, Singapore
Xicheng Jiang, Broadcom, Irvine, CA
Wing Hung Ki, HKUST, Hong Kong, China
Kimmo Koli, Ericsson, Turku, Finland
Jae-Youl Lee, Samsung, Yongin, Korea
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan
Saska Lindfors, Texas Instruments, Helsinki, Finland
Piero Malcovati, University of Pavia, Pavia, Italy
Makoto Nagata, Kobe University, Kobe, Japan
Tim Piessens, ICSense, Leuven, Belgium
Edgar Sanchez-Sinencio, Texas A&M University, College Station, TX
Christoph Sandner, Infineon Technologies Austria, Villach, Austria
Jafar Savoj, Xilinx, San Jose, CA
Ed (Adrianus JM) van Tuijl, University of Twente, Enschede, The Netherlands
Young-Jin Woo, Silicon Works, Daejon, Korea

DATA CONVERTERS SUBCOMMITTEE

Chair: Boris Murmann, Stanford University, Stanford, CA
Brian Brandt, Maxim Integrated Products, North Chelmsford, MA
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Marco Corsi, Texas Instruments, Dallas, TX
Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
John Khoury, Silicon Laboratories, Austin, TX
Stéphane Le Tual, STMicroelectronics, Crolles, France
Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA
Takahiro Miki, Renesas Electronics, Hyogo, Japan
Gerhard Mitterregger, Intel Mobile Communications Austria, St. Magdalen, Austria
Jan Mulder, Broadcom, Bunnik, The Netherlands
Ken Nishimura, Agilent, Santa Clara, CA
Maurits Ortmanns, University of Ulm, Ulm Germany
Shanthi Pavan, Indian Institute Of Technology, Chennai, India
Seung-Tak Ryu, KAIST, Daejon, Korea
Richard Schreier, Analog Devices, Toronto, Canada
Jieh-Tsorng Wu, National Chiao-Tung University, Hsin-Chu, Taiwan

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Chair: Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO
Kazutami Arimoto, Okayama Prefectural University, Okayama, Japan
Wim Dehaene, KU Leuven, Leuven, Belgium
Vasantha Erraguntla, Intel Technology India, Bangalore, India
Takashi Hashimoto, Panasonic, Fukuoka, Japan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Yongha Park, Samsung, Yongin, Korea
Michael Polley, Samsung Mobile, Dallas, TX
Bing Sheu, TSMC, Hsinchu, Taiwan
Kees van Berkel, Ericsson, Eindhoven, The Netherlands
Marian Verhelst, KU Leuven, Leuven, Belgium
Victor Zyuban, IBM T.J. Watson Research Center, Yorktown Heights, NY

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Chair: Stefan Rusu, Intel, Santa Clara, CA
Vivek De, Intel, Hillsboro, OR
Christopher Gonzalez, IBM, Yorktown Heights, NY
Hiroo Hayashi, Toshiba Corporation, Kawasaki, Japan
Anthony Hill, Texas Instruments, Dallas, TX
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Tobias Noll, RWTH Aachen University, Aachen, Germany
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
Luke (Jinuk) Shin, Oracle, Santa Clara, CA
Vladimir Stojanovic, Massachusetts Institute of Technology, Cambridge, MA
Kathy Wilcox, AMD, Boxborough, MA
Se-Hyun Yang, Samsung, Yongin, Korea

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Chair: Roland Thewes, TU Berlin, Berlin, Germany
Ralf Brederlow, Texas Instruments, Freising, Germany
Roman Genov, University of Toronto, Toronto, Canada
Maysam Ghovanloo, Georgia Institute of Technology, Atlanta, GA
Makoto Ikeda, University of Tokyo, Tokyo, Japan
Robert Johansson, OmniVision, Oslo, Norway
Sam Kavusi, Bosch Research and Technology Center, Palo Alto, CA
Tae-Chan Kim, Samsung, Yongin, Kprea
Wentai Liu, UCLA, Los Angeles, CA
Young-Sun Na, LG Electronics, Seoul, Korea
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Yusuke Oike, Sony, Kanagawa, Japan
Aaron Partridge, SiTime, Sunnyvale, CA
Michiel Pertijs, TU Delft, Delft, The Netherlands
Joseph Shor, Intel, Yakum, Israel
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Yong Ping Xu, National University of Singapore, Singapore
Refet Firat Yazicioglu, IMEC, Leuven, Belgium

MEMORY SUBCOMMITTEE

Chair: Kevin Zhang, Intel, Hillsboro, OR
Jonathan Chang, TSMC, Hsinchu, Taiwan
Leland Chang, IBM T. J. Watson Research Center Yorktown Heights, NY
Sungdae Choi, SK hynix, Icheon-si, Korea
Michael Clinton, TSMC Technology, Austin, TX
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Satoru Hanzawa, Hitachi, Tokyo, Japan
Uksong Kang, Samsung Electronics, Hwasung-si, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
Hugh Mair, MediaTek, Fairview, Texas
James Sung, Etron Technology, Hsinchu, Taiwan
Daniele Vimercati, Micron Technology, Agrate, Italy
Tadaaki Yamauchi, Renesas Electronics, Itami, Japan
Takefumi Yoshikawa, Panasonic, Kyoto, Japan

RF SUBCOMMITTEE

Chair: Andreia Cathelin, STMicroelectronics, Crolles, France
Ehsan Afshari, Cornell University, Ithaca, NY
Brian Floyd, North Carolina State University, Raleigh, NC
Chih-Ming Hung, MStar Semiconductor, Taipei, Taiwan
Mike Keaveney, Analog Devices, Limerick, Ireland
Tae Wook Kim, Yonsei University, Seoul, Korea
Antonio Liscidini, University of Toronto, Toronto, Canada
Ahmad Mirzaei, Pennsylvania State University, Unversity Park, PA
Borivoje Nikolic, University of California, Berkeley, CA
Brian Otis, University of Washington, Seattle, WA
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Marc Tiebout, Infineon Technologies Austria, Villach, Austria
Piet Wambacq, imec, Heverlee, Belgium
Taizo Yamawaki, Hitachi, Tokyo, Japan
Masoud Zargari, Qualcomm-Atheros, Irvine, CA
Jing-Hong Zhan, MediaTek, HsinChu, Taiwan

TECHNICAL DIRECTIONS SUBCOMMITTEE

Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Alison Burdett, Toumaz Microsystems, Abingdon, United Kingdom
Eric Colinet, CEA-LETI, Grenoble, France
Jan Genoe, imec, Leuven, Belgium
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Ali Keshavarzi, Cypress,Los Altos, CA
Donghyun Kim, Samsung Techwin, Gyeong, Korea
Tadahiro Kuroda, Keio University, Yokohama, Japan
Shinichiro Mutoh, NTT, Atsugi, Japan
Masaitsu Nakajima, Panasonic, Kyoto, Japan
Chris Nicol, Wave Semiconductor, Sunnyvale, CA
Koichi Nose, Renesas Electronics, Kawasaki, Japan
Pirooz Pavarandeh, Maxim Integrated Products, Sunnyvale, CA
Yogesh K. Ramadass, Texas Instruments, Dallas, TX
David Ruffieux, CSEM, Neuchated, Switzerland
Alice Wang, MediaTek, Austin, TX

WIRELESS SUBCOMMITTEE

Chair: Aarno Pärssinen, Broadcom, Helsinki, Finland
Gangadhar Burra, Texas Instruments, Dallas, TX
Pierre Busson, STMicroelectronics, Crolles, France
Jan Crols, AnSem, Heverlee, Belgium
Hossein Hashemi, University of Southern California, Los Angeles, CA
Myung-Woon Hwang, FCI, Sungnam, Korea
Albert Jerng, Apple, Cupertino, CA
Eric Klumperink, University of Twente, Enschede, The Netherlands
Shouhei Kousai, Toshiba, Kawasaki, Japan
Li Lin, Marvell Semiconductor, Santa Clara, CA
Sven Mattisson, Ericsson, Lund, Sweden
Alyosha Molnar, Cornell University, Ithaca, NY
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Stefano Pellerano, Intel, Hillsboro, OR
Woogeun Rhee, Tsinghua University, Beijing, China
Koji Takinami, Panasonic, Yokohama, Japan
Jan Van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands
Iason Vassiliou, Broadcom, Alimos, Greece

WIRELINE SUBCOMMITTEE

Chair: Daniel Friedman, IBM Thomas J. Watson Research Center, Yorktown Heights, NY
Elad Alon University of California, Berkeley, Berkeley,CA
Ajith Amerasekera, Texas Instruments, Dallas, TX
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Ken Chang, Xilinx, San Jose, CA
SeongHwan Cho, KAIST, Daejon, Korea
Nicola Da Dalt, Infineon, Villach, Austria
Azita Emami, California Institute of Technology, Pasadena, CA
Ichiro Fujimori, Broadcom, Irvine, CA
Pavan Kumar Hanumolu, University of Illinois, Urbana, IL
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Jack Kenney, Analog Devices, Somerset, NJ
Hideyuki Nosaka, NTT Photonics Laboratories, Atsugi, Japan
Frank O'Mahony, Intel, Hillsboro, OR
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan
Koichi Yamaguchi, Renesas Electronics, Kawasaki, Japan

EUROPEAN REGIONAL COMMITTEE

ITPC EUROPEAN REGIONAL CHAIR
Alison Burdett, *Toumaz Microsystems, Abingdon, United Kingdom*

ITPC EUROPEAN REGIONAL VICE CHAIR AND SECRETARY
Maurits Ortmanns, *University of Ulm, Ulm Germany*

Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Ralf Brederlow, Texas Instruments, Freising, Germany
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Pierre Busson, STMicroelectronics, Crolles, France
Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Andreia Cathelin, STMicroelectronics, Crolles, France
Eric Colinet, CEA-LETI, Grenoble, France
Jan Crols, AnSem, Heverlee, Belgium
Nicola Da Dalt, Infineon, Villach, Austria
Wim Dehaene, KU Leuven, Leuven, Belgium
Jan Genoe, imec, Leuven, Belgium
Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands
Robert Johansson, OmniVision, Oslo, Norway
Mike Keaveney, Analog Devices, Limerick, Ireland
Eric Klumperink, University of Twente, Enschede, The Netherlands
Kimmo Koli, ST-Ericsson, Turku, Finland
Stéphane Le Tual, STMicroelectronics, Crolles, France
Saska Lindfors, Texas Instruments, Helsinki, Finland
Piero Malcovati, University of Pavia, Pavia, Italy
Sven Mattisson, Ericsson, Lund, Sweden
Gerhard Mitterregger, Intel Mobile Communications Austria, St. Magdalen, Austria
Jan Mulder, Broadcom, Bunnik, The Netherlands
Tobias Noll, RWTH Aachen University, Aachen, Germany
Aarno Pärssinen, Broadcom, Helsinki, Finland
Michiel Pertijs, TU Delft, Delft, The Netherlands
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Tim Piessens, ICSense, Leuven, Belgium
David Ruffieux, CSEM, Neuchated, Switzerland
Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Christoph Sandner, Infineon Technologies Austria, Villach, Austria

European Members (continued):

Joseph Shor, Intel, Yakum, Israel
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Roland Thewes, TU Berlin, Berlin, Germany
Marc Tiebout, Infineon Technologies, Villach, Austria
Kees van Berkel, Ericsson, Eindhoven, The Netherlands
Jan Van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands
Ed van Tuijl, University of Twente, Enschede, The Netherlands
Iason Vassiliou, Broadcom, Alimos, Greece
Marian Verhelst, KU Leuven, Leuven, Belgium
Daniele Vimercati, Micron Technology, Agrate, Italy
Piet Wambacq, imec, Heverlee, Belgium
Refet Firat Yazicioglu, imec, Leuven, Belgium

FAR EAST REGIONAL COMMITTEE

ITPC FAR EAST REGIONAL CHAIR

Kazutami Arimoto, Okayama Prefectural University, Okayama, Japan

ITPC FAR EAST REGIONAL VICE-CHAIR

Jae-Youl Lee, Samsung, Yongin, Korea

ITPC FAR EAST REGIONAL SECRETARY

Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan

Jonathan Chang, TSMC, Hsinchu, Taiwan
SeongHwan Cho, KAIST, Daejon, Korea
Sungdae Choi, SK hynix, Icheon-si, Korea
Vasantha Erraguntla, Intel Technology India, Bangalore, India
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Satoru Hanzawa, Hitachi, Tokyo, Japan
Takashi Hashimoto, Panasonic, Fukuoka, Japan
Hiroo Hayashi, Toshiba, Kawasaki, Japan
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Chih-Ming Hung, MStar Semiconductor, Taipei, Taiwan
Myung-Woon Hwang, FCI, Sungnam, Korea
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
Makoto Ikeda, University of Tokyo, Tokyo, Japan
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Minkyu Je, Institute of Microelectronics, A*STAR, Singapore
Albert Jerng, Apple, Cupertino, CA
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Uksong Kang, Samsung Electronics, Hwasung, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Wing Hung Ki, HKUST, Hong Kong, China
Chulwoo Kim, Korea University, Seoul, Korea
Donghyun Kim, Samsung Techwin, Gyeong, Korea
Tae-Chan Kim, Samsung, Yongin, Korea
Tae Wook Kim, Yonsei University, Seoul, Korea
Shouhei Kousai, Toshiba, Kawasaki, Japan
Tadahiro Kuroda, Keio University, Yokohama, Japan
Takahiro Miki, Renesas Electronics, Itami, Japan
Shinichiro Mutoh, NTT, Atsugi, Japan
Young-Sun Na, LG Electronics, Seoul, Korea
Makoto Nagata, Kobe University, Kobe, Japan
Masaitsu Nakajima, Panasonic, Kyoto, Japan
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Hideyuki Nosaka, NTT Photonics Laboratories, Atsugi, Japan
Koichi Nose, Renesas Electronics, Kawasaki, Japan
Yusuke Oike, Sony, Atsugi, Japan
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Yongha Park, Samsung, Yongin, Korea
Shanthi Pavan, Indian Institute of Technology Madras, Chennai, India
Woogeun Rhee, Tsinghua University, Beijing, China
Seung-Tak Ryu, KAIST, Daejon, Korea
Bing Sheu, TSMC, Hsinchu, Taiwan
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
James Sung, Etron Technology, Hsinchu, Taiwan
Koji Takinami, Panasonic, Yokohama, Japan
Young-Jin Woo, Silicon Works, Daejon, Korea
Jieh-Tsorng Wu, National Chiao-Tung University, Hsinchu, Taiwan
Yong Ping Xu, National University of Singapore, Singapore
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan
Koichi Yamaguchi, Renesas Electronics, Kawasaki, Japan
Tadaaki Yamauchi, Renesas Electronics, Itami, Japan
Taizo Yamawaki, Hitachi, Tokyo, Japan
Se-Hyun Yang, Samsung, Yongin-Si, Korea
Takefumi Yoshikawa, Panasonic, Kyoto, Japan
Jing-Hong Zhan, MediaTek, Hsinchu, Taiwan

HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2014 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2014". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2014 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday, February 8	4:00 pm to 7:00 pm
Sunday, February 9	6:30 am to 8:30 pm
Monday, February 10	6:30 am to 3:00 pm
Tuesday, February 11	8:00 am to 3:00 pm
Wednesday, February 12	8:00 am to 3:00 pm
Thursday, February 13	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 10, 2014.** After January 10th, and on or before 11:59 pm Pacific Time Monday January 20, 2014, registrations will be processed **at the Late Registration rates. After January 20th, you must register on site at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Monday January 20, 2014,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 20, 2014.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE Membership Saves on ISSCC Registration

Take advantage of reduced ISSCC fees by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

SSCS Membership – a Valuable Professional Resource for your Career Growth

Membership in the Solid-State Circuit Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuit Society where you can:

-Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid-State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and member-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. New publications included in your SSCS membership are the RFIC Virtual Journal and the Journal on Exploratory Solid-State Computational Devices and Circuits, a new open access publication due for initial publication in mid 2014.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will receive an exclusive benefit of a $40 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuit Society today at sscs.ieee.org – you will not want to miss out on the opportunity and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available each evening starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC LED Flashlight: A convenient crank-powered LED flashlight will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed during registration hours beginning on Sunday at 10:00 am. If you do not want the Digest book (you still get the download), a registration credit of $10 is offered.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions and an ID/password will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2014 for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four

additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to hear from an accomplished speaker, get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. This event is open to women only at a discounted fee.

OPTIONAL PUBLICATIONS

ISSCC 2014 Publications: The following ISSCC 2014 publications can be purchased in advance or on site:

2014 ISSCC Download USB: All of the downloads included in conference registration **(mailed in March).**

2014 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**

2014 Short Course DVD: "Biomedical and Sensor Interface Circuits" **(mailed in May)**.

Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVD contains a pdf file of the presentations suitable for printing, and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the order form for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $235 for a single/double, $255 for a triple and $275 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2014 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 20, 2014 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 20th, the group rates may no longer be available and reservations will be filled at the best available rate.**

Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

REFERENCE INFORMATION

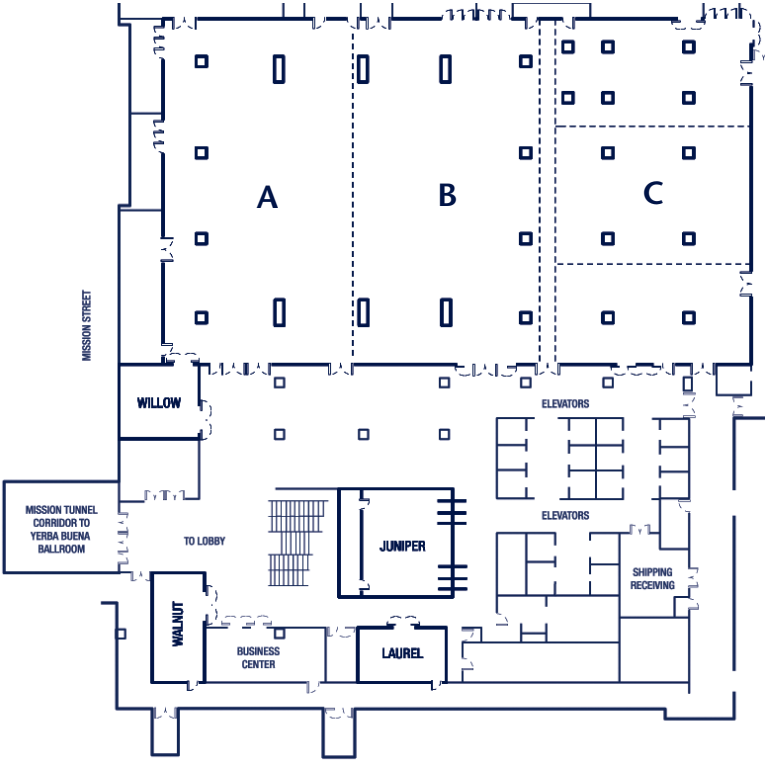
TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registrationquestions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 55 Fourth Street San Francisco, CA 94103
Press Information:	Kenneth C. Smith Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com

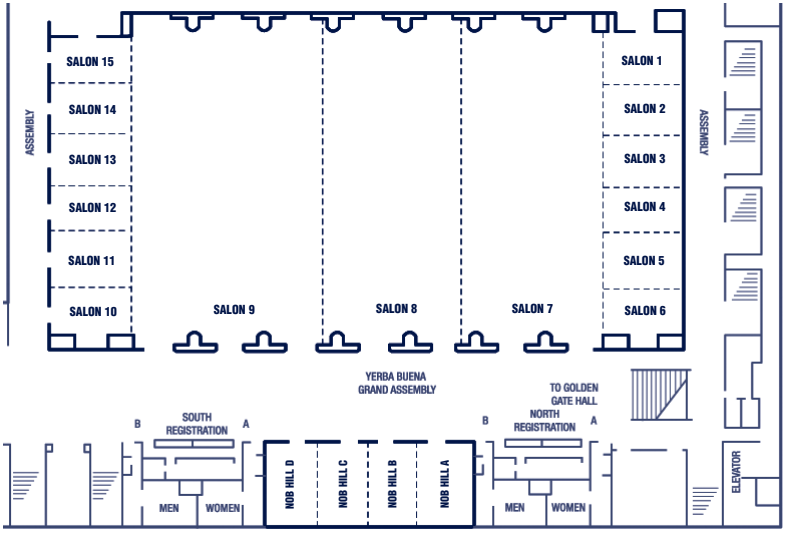
Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2015 will be held on February 22-26, 2015 at the San Francisco Marriott Marquis Hotel.

Golden Gate Ballroom



Yerba Buena Ballroom



IEEE

445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

ISSCC.org

sscs.ieee.org

ISSCC 2014 ADVANCE PROGRAM